



2024 07

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(Fax) 010-62600826





		3C5000L
		V1.2



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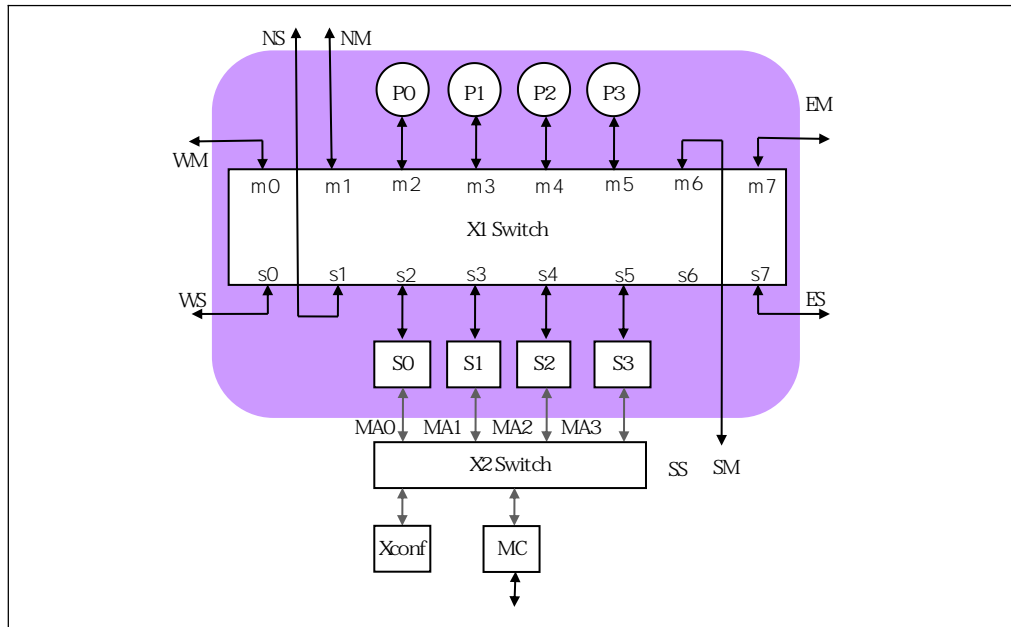
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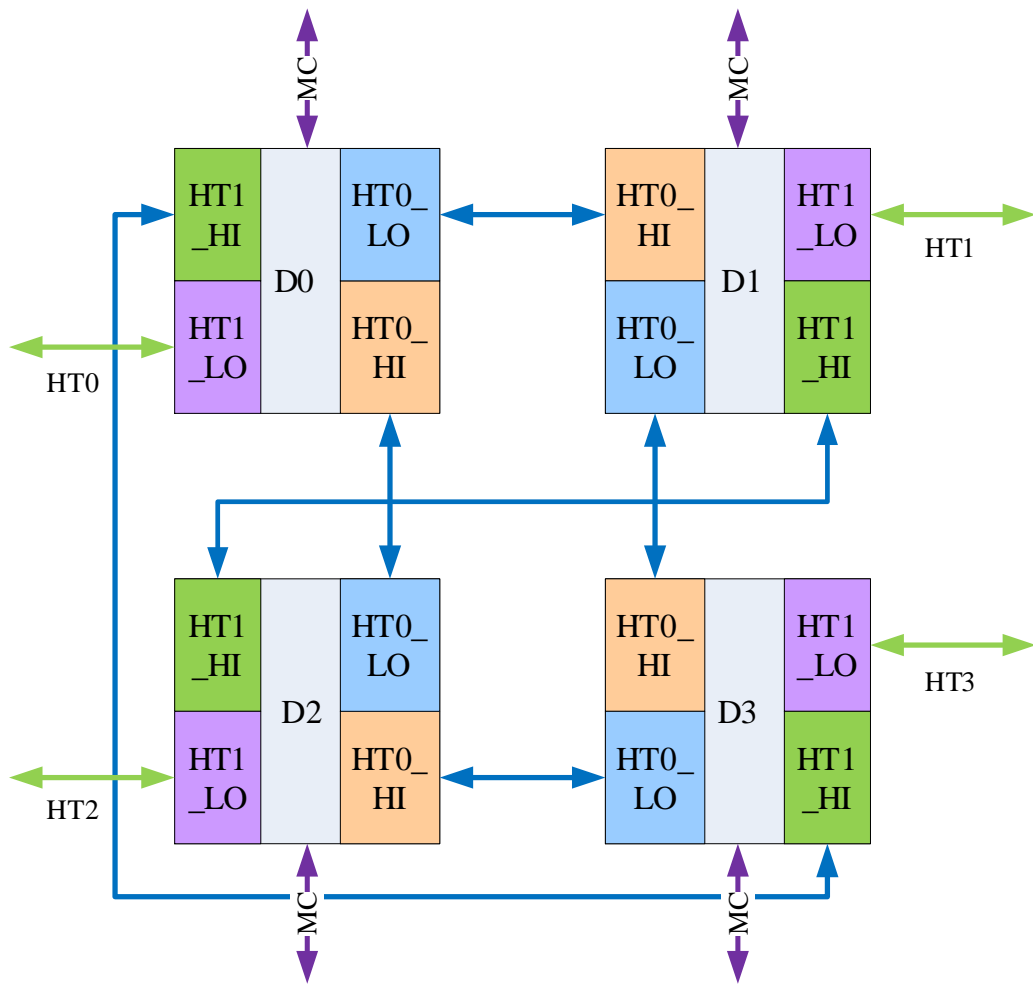


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3C5000L

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	PLL	4.8-6.4GHz																														
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	PLL	4.8-6.4GHz																														
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	HT1-hi																															
	HT1-lo																															
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	D2_HT1_hi																															
	D2_HT1_lo																															
	D3_HT1_hi																															
	D3_HT1_lo																															

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0	0	0	0x0000_0000_0000	0x0FFF_FFFF_FFFF
	1	1	0x1000_0000_0000	0x1FFF_FFFF_FFFF
	2	2	0x2000_0000_0000	0x2FFF_FFFF_FFFF
	3	3	0x3000_0000_0000	0x3FFF_FFFF_FFFF
1	4	4	0x4000_0000_0000	0x4FFF_FFFF_FFFF
	5	5	0x5000_0000_0000	0x5FFF_FFFF_FFFF
	6	6	0x6000_0000_0000	0x6FFF_FFFF_FFFF
	7	7	0x7000_0000_0000	0x7FFF_FFFF_FFFF
2	8	8	0x8000_0000_0000	0x8FFF_FFFF_FFFF
	9	9	0x9000_0000_0000	0x9FFF_FFFF_FFFF
	10	10	0xA000_0000_0000	0xAFFF_FFFF_FFFF
	11	11	0xB000_0000_0000	0xBFFF_FFFF_FFFF
3	12	12	0xC000_0000_0000	0xCFFF_FFFF_FFFF
	13	13	0xD000_0000_0000	0xDFFF_FFFF_FFFF
	14	14	0xE000_0000_0000	0xEFFF_FFFF_FFFF
	15	15	0xF000_0000_0000	0xFFFF_FFFF_FFFF



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4'h3	13:12	4'hb	29:28
4'h4	15:14	4'hc	31:30
4'h5	17:16	4'hd	33:32
4'h6	19:18	4'he	35:34
4'h7	21:20	4'hf	37:36

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[7]	[6]	[5]	[4]
	SCACHE/		

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0x2000	CORE0_WIN0_BASE	0x2100	CORE1_WIN0_BASE
0x2008	CORE0_WIN1_BASE	0x2108	CORE1_WIN1_BASE
0x2010	CORE0_WIN2_BASE	0x2110	CORE1_WIN2_BASE
0x2018	CORE0_WIN3_BASE	0x2118	CORE1_WIN3_BASE
0x2020	CORE0_WIN4_BASE	0x2120	CORE1_WIN4_BASE
0x2028	CORE0_WIN5_BASE	0x2128	CORE1_WIN5_BASE
0x2030	CORE0_WIN6_BASE	0x2130	CORE1_WIN6_BASE
0x2038	CORE0_WIN7_BASE	0x2138	CORE1_WIN7_BASE
0x2040	CORE0_WIN0_MASK	0x2140	CORE1_WIN0_MASK
0x2048	CORE0_WIN1_MASK	0x2148	CORE1_WIN1_MASK
0x2050	CORE0_WIN2_MASK	0x2150	CORE1_WIN2_MASK
0x2058	CORE0_WIN3_MASK	0x2158	CORE1_WIN3_MASK
0x2060	CORE0_WIN4_MASK	0x2160	CORE1_WIN4_MASK
0x2068	CORE0_WIN5_MASK	0x2168	CORE1_WIN5_MASK
0x2070	CORE0_WIN6_MASK	0x2170	CORE1_WIN6_MASK
0x2078	CORE0_WIN7_MASK	0x2178	CORE1_WIN7_MASK
0x2080	CORE0_WIN0_MMAP	0x2180	CORE1_WIN0_MMAP
0x2088	CORE0_WIN1_MMAP	0x2188	CORE1_WIN1_MMAP
0x2090	CORE0_WIN2_MMAP	0x2190	CORE1_WIN2_MMAP
0x2098	CORE0_WIN3_MMAP	0x2198	CORE1_WIN3_MMAP
0x20a0	CORE0_WIN4_MMAP	0x21a0	CORE1_WIN4_MMAP
0x20a8	CORE0_WIN5_MMAP	0x21a8	CORE1_WIN5_MMAP
0x20b0	CORE0_WIN6_MMAP	0x21b0	CORE1_WIN6_MMAP
0x20b8	CORE0_WIN7_MMAP	0x21b8	CORE1_WIN7_MMAP
0x2200	CORE2_WIN0_BASE	0x2300	CORE3_WIN0_BASE



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0x2208	CORE2_WIN1_BASE	0x2308	CORE3_WIN1_BASE
0x2210	CORE2_WIN2_BASE	0x2310	CORE3_WIN2_BASE
0x2218	CORE2_WIN3_BASE	0x2318	CORE3_WIN3_BASE

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0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP
0x24b8	SCACHE0_WIN7_MMAP	0x25b8	SCACHE1_WIN7_MMAP
0x2600	SCACHE2_WIN0_BASE	0x2700	SCACHE3_WIN0_BASE
0x2608	SCACHE2_WIN1_BASE	0x2708	SCACHE3_WIN1_BASE
0x2610	SCACHE2_WIN2_BASE	0x2710	SCACHE3_WIN2_BASE
0x2618	SCACHE2_WIN3_BASE	0x2718	SCACHE3_WIN3_BASE
0x2620	SCACHE2_WIN4_BASE	0x2720	SCACHE3_WIN4_BASE
0x2628	SCACHE2_WIN5_BASE	0x2728	SCACHE3_WIN5_BASE
0x2630	SCACHE2_WIN6_BASE	0x2730	SCACHE3_WIN6_BASE
0x2638	SCACHE2_WIN7_BASE	0x2738	SCACHE3_WIN7_BASE
0x2640	SCACHE2_WIN0_MASK	0x2740	SCACHE3_WIN0_MASK
0x2648	SCACHE2_WIN1_MASK	0x2748	SCACHE3_WIN1_MASK
0x2650	SCACHE2_WIN2_MASK	0x2750	SCACHE3_WIN2_MASK
0x2658	SCACHE2_WIN3_MASK	0x2758	SCACHE3_WIN3_MASK
0x2660	SCACHE2_WIN4_MASK	0x2760	SCACHE3_WIN4_MASK
0x2668	SCACHE2_WIN5_MASK	0x2768	SCACHE3_WIN5_MASK
0x2670	SCACHE2_WIN6_MASK	0x2770	SCACHE3_WIN6_MASK
0x2678	SCACHE2_WIN7_MASK	0x2778	SCACHE3_WIN7_MASK
0x2680	SCACHE2_WIN0_MMAP	0x2780	SCACHE3_WIN0_MMAP
0x2688	SCACHE2_WIN1_MMAP	0x2788	SCACHE3_WIN1_MMAP
0x2690	SCACHE2_WIN2_MMAP	0x2790	SCACHE3_WIN2_MMAP
0x2698	SCACHE2_WIN3_MMAP	0x2798	SCACHE3_WIN3_MMAP
0x26a0	SCACHE2_WIN4_MMAP	0x27a0	SCACHE3_WIN4_MMAP
0x26a8	SCACHE2_WIN5_MMAP	0x27a8	SCACHE3_WIN5_MMAP
0x26b0	SCACHE2_WIN6_MMAP	0x27b0	SCACHE3_WIN6_MMAP
0x26b8	SCACHE2_WIN7_MMAP	0x27b8	SCACHE3_WIN7_MMAP
-	-	0x2900	IO_L2X_WIN0_BASE
-	-	0x2908	IO_L2X_WIN1_BASE
-	-	0x2910	IO_L2X_WIN2_BASE
-	-	0x2918	IO_L2X_WIN3_BASE

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-	-	0x2920	IO_L2X_WIN4_BASE
-	-	0x2928	IO_L2X_WIN5_BASE
-	-	0x2930	IO_L2X_WIN6_BASE
-	-	0x2938	IO_L2X_WIN7_BASE
-	-	0x2940	IO_L2X_WIN0_MASK
-	-	0x2948	IO_L2X_WIN1_MASK
-	-	0x2950	IO_L2X_WIN2_MASK
-	-	0x2958	IO_L2X_WIN3_MASK
-	-	0x2960	IO_L2X_WIN4_MASK
-	-	0x2968	IO_L2X_WIN5_MASK
-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-	0x2998	IO_L2X_WIN3_MMAP
-	-	0x29a0	IO_L2X_WIN4_MMAP
-	-	0x29a8	IO_L2X_WIN5_MMAP
-	-	0x29b0	IO_L2X_WIN6_MMAP
-	-	0x29b8	IO_L2X_WIN7_MMAP
0x2a00	HT0_LO_WIN0_BASE	0x2b00	HT0_HI_WIN0_BASE
0x2a08	HT0_LO_WIN1_BASE	0x2b08	HT0_HI_WIN1_BASE
0x2a10	HT0_LO_WIN2_BASE	0x2b10	HT0_HI_WIN2_BASE
0x2a18	HT0_LO_WIN3_BASE	0x2b18	HT0_HI_WIN3_BASE
0x2a20	HT0_LO_WIN4_BASE	0x2b20	HT0_HI_WIN4_BASE
0x2a28	HT0_LO_WIN5_BASE	0x2b28	HT0_HI_WIN5_BASE
0x2a30	HT0_LO_WIN6_BASE	0x2b30	HT0_HI_WIN6_BASE
0x2a38	HT0_LO_WIN7_BASE	0x2b38	HT0_HI_WIN7_BASE
0x2a40	HT0_LO_WIN0_MASK	0x2b40	HT0_HI_WIN0_MASK
0x2a48	HT0_LO_WIN1_MASK	0x2b48	HT0_HI_WIN1_MASK
0x2a50	HT0_LO_WIN2_MASK	0x2b50	HT0_HI_WIN2_MASK
0x2a58	HT0_LO_WIN3_MASK	0x2b58	HT0_HI_WIN3_MASK
0x2a60	HT0_LO_WIN4_MASK	0x2b60	HT0_HI_WIN4_MASK
0x2a68	HT0_LO_WIN5_MASK	0x2b68	HT0_HI_WIN5_MASK
0x2a70	HT0_LO_WIN6_MASK	0x2b70	HT0_HI_WIN6_MASK
0x2a78	HT0_LO_WIN7_MASK	0x2b78	HT0_HI_WIN7_MASK
0x2a80	HT0_LO_WIN0_MMAP	0x2b80	HT0_HI_WIN0_MMAP
0x2a88	HT0_LO_WIN1_MMAP	0x2b88	HT0_HI_WIN1_MMAP



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0x2e38	HT1_LO_WIN7_BASE	0x2f38	HT1_HI_WIN7_BASE
0x2e40	HT1_LO_WIN0_MASK	0x2f40	HT1_HI_WIN0_MASK
0x2e48	HT1_LO_WIN1_MASK	0x2f48	HT1_HI_WIN1_MASK
0x2e50	HT1_LO_WIN2_MASK	0x2f50	HT1_HI_WIN2_MASK
0x2e58	HT1_LO_WIN3_MASK	0x2f58	HT1_HI_WIN3_MASK
0x2e60	HT1_LO_WIN4_MASK	0x2f60	HT1_HI_WIN4_MASK
0x2e68	HT1_LO_WIN5_MASK	0x2f68	HT1_HI_WIN5_MASK
0x2e70	HT1_LO_WIN6_MASK	0x2f70	HT1_HI_WIN6_MASK
0x2e78	HT1_LO_WIN7_MASK	0x2f78	HT1_HI_WIN7_MASK
0x2e80	HT1_LO_WIN0_MMAP	0x2f80	HT1_HI_WIN0_MMAP
0x2e88	HT1_LO_WIN1_MMAP	0x2f88	HT1_HI_WIN1_MMAP
0x2e90	HT1_LO_WIN2_MMAP	0x2f90	HT1_HI_WIN2_MMAP
0x2e98	HT1_LO_WIN3_MMAP	0x2f98	HT1_HI_WIN3_MMAP
0x2ea0	HT1_LO_WIN4_MMAP	0x2fa0	HT1_HI_WIN4_MMAP
0x2ea8	HT1_LO_WIN5_MMAP	0x2fa8	HT1_HI_WIN5_MMAP
0x2eb0	HT1_LO_WIN6_MMAP	0x2fb0	HT1_HI_WIN6_MMAP
0x2eb8	HT1_LO_WIN7_MMAP	0x2fb8	HT1_HI_WIN7_MMAP

3- 7MMAP

[63:48]	[47 10]	[7 4]	[3 0]

3- 8

0-3	Scache0-3
4-5	MC0-1
a	HT0_lo
b	HT0_hi
c	SE
d	MISC

e	HT1_lo
f	HT1_hi

3- 9 MMAP

[7]	[6]	[5]	[4]
	DDR interleave_bit CSR0x0400	0	
	10		

4- 1

7:0	Version	R	8'h11	

4- 2

0	Centigrade	R	1'b1	1	CSR[0x428]
1	Node counter	R	1'b1	1	CSR[0x408]
2	MSI	R	1'b1	1	MSI
3	EXT_IOI	R	1'b1	1	EXT_IOI
4	IPI_percore	R	1'b1	1 IPI	CSR
5	Freq_percore	R	1'b1	1	CSR
6	Freq_scale	R	1'b1	1	
7	DVFS_v1	R	1'b1	1	v1
8	Tsensor	R	1'b1	1	

9		R	1'b1	
10		R	1'b0	
11	Guest Mode	WR	1'b0	KVM

4- 3

63:0	Vendor	R	0x6e6f7367_6e6f6f4c	Loongson
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4- 4

63:0	ID	R	0x00003030_30354133	3A5000
------	----	---	---------------------	--------

4- 5

0		RW	1'b0	
1		RW	1'b0	
3:2		RW	2'b0	
4	MCO_disable_confspace	RW	1'b0	MCO DDR
5	MCO_default_confspace	RW	1'b1	
6	MCA0 clock en	RW	1'b1	MCA0
7	MCO_resetrn	RW	1'b1	MCO
8	MCO_clken	RW	1'b1	MCO
9	MC1_disable_confspace	RW	1'b0	MC1 DDR
10	MC1_default_confspace	RW	1'b1	
11	MCA1 clock en	RW	1'b1	MCA1
12	MC1_resetrn	RW	1'b1	MC1

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13	MC1_clken	RW	1'b1	MC1
26:24	HT0_freq_scale_ctrl	RW	3'b011	HT 0
27	HT0_clken	RW	1'b1	HT0
30:28	HT1_freq_scale_ctrl	RW	3'b011	HT 1
31	HT1_clken	RW	1'b1	HT1
42:40	Node_freq_ctrl	RW	3'b111	
43	-	RW	1'b1	
63:56	Cpu_version	R	2'h3D	CPU

4- 6

Address Range	Register Name	Access	Value	Function
15:0				
19:16	HTsideband	RW	2'b0	HT
23:20	I2C	RW	2'b0	I2C
27:24	UART	RW	2'b0	UART
31:28	SPI	RW	2'b0	SPI
35:32	GPIO	RW	2'b0	GPIO
39:36	SE UART	RW	2'b0	SE UART
43:40	SE SPI	RW	2'b0	SE SPI
47:44	SE I2C	RW	2'b0	SE I2C
51:48	SE SCI	RW	2'b0	SE SCI
55:52	SE RNG	RW	2'b0	SE RNG
59:56	SE GPIO	RW	2'b0	SE GPIO

4- 7

Address Range	Register Name	Access	Value	Function
31:0		R		
37:32	Chip_config	R		
47:38	Sys_clkseli	R		
55:48	Bad_ip_core	R		core7-core0

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57:56	Bad_ip_ddr	R		2	DDR
61:60	Bad_ip_ht	R		2	HT

4- 8

15:0		R			
19:16		R			
20	dotest	R			Dotest
21	iccc_en	R			Iccc_en
23:22		R			
24	Thsens0_overflow	R			0
25	Thsens1_overflow	R			1
31:26					
47:32	Thsens0_out	R			0 =Thsens0_out * 731 / 0x4000 - 273 -40 - 125
63:48	Thsens1_out	R			1 =Thsens1_out * 731 / 0x4000 - 273 -40 - 125

4- 9

0	SEL_PLL_NODE	RW	0x0	1 Node PLL 0 Node SYS CLOCK
1		RW	0x0	
2	SOFT_SET_PLL	RW	0x0	PLL
3	BYPASS_L1	RW	0x0	Bypass L1 PLL
7:4	-	RW	0x0	
8	VDDA_LDO_EN	RW	0x0	VDDA LDO
9	VDDD_LDO_EN	RW	0x0	VDDD LDO
11:10	-			
12	DACPD_L2	RW	0x0	L2 DACPD
13	DSMPD_L2	RW	0x0	L2 DSMPD
15:14		RW	0x0	
16	LOCKED_L1	R	0x0	L1 PLL
18:17	-	R	0x0	
19	PD_L1	RW	0x0	L1 PLL
21:20		RW	0x0	
22	L2_SEL	RW	0x0	L2
25:23		RW	0x0	
31:26	L1_DIV_REFC	RW	0x1	L1 PLL
40:32	L1_DIV_LOOPC	RW	0x1	L1 PLL
41				
47:42	L1_DIV_OUT	RW	0x1	L1 PLL
53:48	L2_DIV_REFC	RW		
63:54	L2_DIV_LOOPC	RW		

69:64	L2_DIV_OUT	RW		
95:70	-	RW		
119:96	L2_FRAC	RW		
122:120	VDDA_LDO_CTRL	RW		
123	VDDA_LDO_BYPASS	RW		
126:124	VDDD_LDO_CTRL	RW		
127:124	VDDD_LDO_BYPASS	RW		
	-	RW		

4- 10

[0]	SEL_MEM_PLL	RW	0x0	1 MEM PLL 0 MEM SYS CLOCK
[1]	SOFT_SET_MEM_PLL	RW	0x0	MEM PLL
[2]	BYPASS_MEM_PLL	RW	0x0	Bypass MEM_PLL
[3]	MEMDIV_RESETh	RW	0x1	
[5:4]	MEMDIV_MODE	RW		00 01 2 10 4 11
[6]	LOCKED_MEM_PLL	R	0x0	MEM_PLL
[7]	PD_MEM_PLL	RW	0x0	MEM PLL
[13:8]	MEM_PLL_DIV_REFC	RW	0x1	MEM PLL NODE NODE_CLOCK_SEL 1
[23:14]	MEM_PLL_DIV_LOOPC	RW	0x41	MEM PLL
[29:24]	MEM_PLL_DIV_OUT	RW	0x0	MEM PLL
[30]	NODE_CLOCK_SEL	RW	0x0	0 MEM_PLL MEM 1 NODE_CLOCK
[31]	-			

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[34:32]	VDDA_LDO_CTRL	RW		
[35]	VDDA_LDO_BYPASS	RW		
[38:36]	VDDD_LDO_CTRL	RW		
[39]	VDDD_LDO_BYPASS	RW		
[40]	VDDA_LDO_EN	RW		
[41]	VDDD_LDO_EN	RW		
		RW		

4- 11

Field	Register	Access	Mask	Value
2:0	core0_freqctrl	RW	0x7	0
3	core0_en	RW	0x1	0
6:4	core1_freqctrl	RW	0x7	1
7	core1_en	RW	0x1	1
10:8	core2_freqctrl	RW	0x7	2
11	core2_en	RW	0x1	2
14:12	core3_freqctrl	RW	0x7	3
15	core3_en	RW	0x1	3
			:	+1 /8

4- 12

Field	Register	Access	Mask	Value
0	Core0_resetrn_pre	RW	0x1	0
1	Core0_resetrn	RW	0x1	0
2	Core1_resetrn_pre	RW	0x1	1

3	Core1_resetrn	RW	0x1	1
4	Core2_resetrn_pre	RW	0x1	2
5	Core2_resetrn	RW	0x1	2
6	Core3_resetrn_pre	RW	0x1	3
7	Core3_resetrn	RW	0x1	3

4- 13

3:0	scid_sel	RW	0x0	
7:4	Node_mask	RW	0xF	
8	xrouter_en	RW	0x0	HT1
9	disable_0x3ff0	RW	0x0	0x3ff0_0000
10	Fast_path_36_en	RW	0x0	36 8
11	Fast_path_27_en	RW	0x0	27 8
12	mcc_en	RW	0x0	MCC
14	Scahe_1MB	RW		Scache
19:16	ccsd_id	RW	0x0	
24	ccsd_en	RW	0x0	
31:30	mc_en	RW	0x3	MC
37:32	interleave_bit	RW	0x0	
39	interleave_en	RW	0x0	
43:40	ht_control	R		Ht
47:44	ht_reg_disable	RW	0x0	ht HT HT
60:56	Line_ag_cfg	RW	0x0	

4- 14

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46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock
48	EXT_INT_en	RW	0x0	IO
49	INT_encode	RW	0x0	
53:52				
54				
57:56	thsensor_sel	RW	0x0	
62:60	Auto_scale	R	0x0	
63	Auto_scale_doing	R	0x0	

4- 15

7:0	Centigrade temperature	RO	0x0	
63:8		RW	0x0	

4- 16 SRAM

31:0	sram_ctrl	RW	0x0	Sram
63:32		RW	0x0	

4- 17 FUSE

127:0	Fuse_0	RW	0x0	
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4- 18 FUSE

4- 18 FUSE				
127:0	Fuse_1	RW	OxO	

5- 1

Boot Clock	SYS_CLOCK	* 1			SPI UART I2C
Main Clock	SYS PLL	PLL			SYS PLL Node Clock Core Clock HTcore Clock IA132 Clock Mem Clock Stable Clock
Node Clock	Main Clock	* 1			HT
Core0 Clock	Main Clock	* 1			Core0
Core1 Clock	Main Clock	* 1			Core1
Core2 Clock	Main Clock	* 1			Core2
Core3 Clock	Main Clock	* 1			Core3
HTcore0 Clock	Node Clock	* 1			HT0 1GHz
HTcore1 Clock	Node Clock	* 1			HT1 1GHz

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IA132 Clock	Main Clock	* 1			IA132 1GHz
Stable Clock	SYS_CLOCK	* 1			
Mem Clock	MEM PLL	PLL			
	Main Clock	/2 /4 /8			

5- 2

Field	Register	Access	Mask	Value
2:0	core0_freqctrl	RW	0x7	0
3	core0_en	RW	0x1	0
6:4	core1_freqctrl	RW	0x7	1
7	core1_en	RW	0x1	1
10:8	core2_freqctrl	RW	0x7	2
11	core2_en	RW	0x1	2
14:12	core3_freqctrl	RW	0x7	3
15	core3_en	RW	0x1	3
			:	+1 /8

5- 3

Field	Register	Access	Mask	Value
35:32	freqscale_mode_core	RW	0x0	

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				Q: (n+1)/8 I: 1/(n+1)
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5- 4

22	freqscale_percore	RW	OxO	
23	clken_percore	RW	OxO	

5- 5

4	freqscale_mode	RW	OxO	Q: (n+1)/8 I: 1/(n+1)
3	clken	RW	OxO	
2:0	freqscale	RW	OxO	

5- 6

5- 6				
42:40	Node0_freq_ctrl	RW	3'b111	0

5- 7

5- 7				
36	freqscale_mode_node	RW	0x0	0: (n+1)/8 1: 1/(n+1)



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26:24	HIO_freq_scale_ctrl	RW	3'b111	HT	0
27	HIO_clken	RW	1'b1		HIO
30:28	HT1_freq_scale_ctrl	RW	3'b111	HT	1
31	HT1_clken	RW	1'b1		HT1

5- 10

39:38	freqscale_mode_HT	RW	0x0	HT	0: (n+1)/8 1: 1/(n+1)
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5- 11

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0 Stable clock
40	freqscale_mode_stable	RW	0x0	0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	S

35
ab

5- 12 GPIO

31:0	GPIO_OEn	RW	32'hfffffff	GPIO
63:32	GPIO_FUNC_En	RW	32'hfff0000	GPIO

6- 1

Core0_timer_config	0x1060	RW	0
Core0_timer_ticks	0x1070	R	0
Core1_timer_config	0x1160	RW	1
Core1_timer_ticks	0x1170	R	1
Core2_timer_config	0x1260	RW	2
Core2_timer_ticks	0x1270	R	2
Core3_timer_config	0x1360	RW	3
Core3_timer_ticks	0x1370	R	3

6- 2

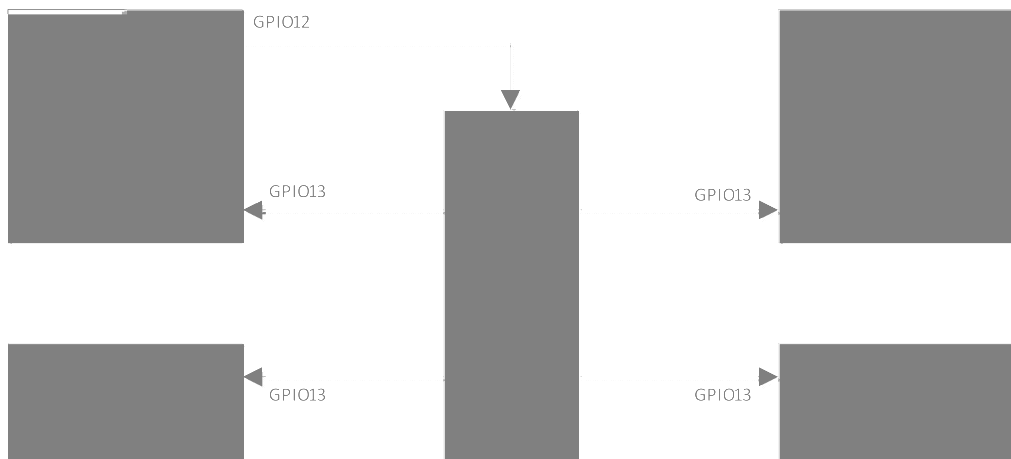
percore_timer_config	0x1060	RW	
percore_timer_ticks	0x1070	R	

6- 3

timer_config				
63	1	RW	0x1	1 1
62	Periodic	RW	0x0	timer_config InitVal 1 0
61	Enable	RW	0x0	1
47:0	InitVal	RW	0x0	
timer_ticks				
63:48	0	R	0x0	0
47:0	Ticks	R	0x0	48'hffff_fff_fff

6- 4

20	stable_sel	RW	0x0	0 SYS CLOCK 1 NODE CLOCK
21	stable_reset	RW	0x0	1 0
40	freqscale_mode_stable	RW	0x0	Stable clock 0: (n+1)/8 1: 1/(n+1)
46:44	freqscale_stable	RW	0x0	Stable clock
47	clken_stable	RW	0x0	Stable clock



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7- 1

31:0	GPIO_OEn	RW	32'hfffffff	GPIO
63:32	GPIO_FUNC_En	RW	32'hffff0000	GPIO

7- 2

31:0	GPIO_O	RW	32'h0	GPIO
63:32	GPIO_I	RO	32'h0	GPIO

7- 3

31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0 - 1 -
63:32	GPIO_INT_en	RW	32'h0	GPIO



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7- 5

31:0	GPIO_INT_Pol	RW	32'h0	GPIO 0-



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				1 -
63:32	GPIO_INT_en	RW	32'h0	GPIO



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8- 1





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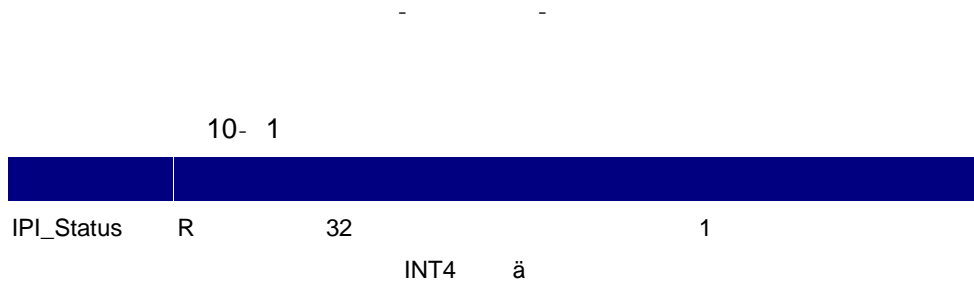
Slock1_valid	0x0208	[63:63]	1
Slock1_addr	0x0208	[47:0]	1
Slock1_mask	0x0248	[47:0]	1
Slock2_valid	0x0210	[63:63]	2
Slock2_addr	0x0210	[47:0]	2
Slock2_mask	0x0250	[47:0]	2
Slock3_valid	0x0218	[63:63]	3
Slock3_addr	0x0218	[47:0]	3
Slock3_mask	0x0258	[47:0]	3

9- 2 Cache SC_CONFIG

Cache SC_CONFIG				
0	LRU en	RW	1'b1	Scache LRU
16	Prefetch En	RW	1'b1	Scache
22:20	Prefetch config	RW	3'h1	scache 0- 4KB 1- 16KB 2- 64KB 3- 1MB 7- SCID_SEL==0
26:24	Prefetch lookahead	RW	3'h2	scache 0- 1- 0x100 2- 0x200 3- 0x300 4- 0x400 5- 0x500 6- 0x600 7- 0x700 SCID_SEL==0
30:28	Sc stall dirq cycle	RW	3'h2	SC dirq 0- 1 cycle nonstall 1- 16-31 cycle random 2- 32-63 cycle random

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				3- 64-127 cycle random 4- 128-255 cycle random -
31	MCC storefill en	RW	1'b0	MCC storefill
34:32				
35	MCC clean exclusive replace en	RW	1'b0	
36	MCC clean shared replace en	RW	1'b0	



Core0_IPI_Enalbe	0x1004	RW	0	IPI_Enalbe
Core0_IPI_Set	0x1008	W	0	IPI_Set
Core0_IPI_Clear	0x100c	W	0	IPI_Clear
Core0_MailBox0	0x1020	RW	0	IPI_MailBox0
Core0_MailBox1	0x1028	RW	0	IPI_MailBox1
Core0_MailBox2	0x1030	RW	0	IPI_MailBox2
Core0_MailBox3	0x1038	RW	0	IPI_MailBox3

10- 3 1

Core1_IPI_Status	0x1100	R	1	IPI_Status
Core1_IPI_Enalbe	0x1104	RW	1	IPI_Enalbe
Core1_IPI_Set	0x1108	W	1	IPI_Set
Core1_IPI_Clear	0x110c	W	1	IPI_Clear
Core1_MailBox0	0x1120	R	1	IPI_MailBox0
Core1_MailBox1	0x1128	RW	1	IPI_MailBox1
Core1_MailBox2	0x1130	W	1	IPI_MailBox2
Core1_MailBox3	0x1138	W	1	IPI_MailBox3

10- 4 2

Core2_IPI_Status	0x1200	R	2	IPI_Status
Core2_IPI_Enalbe	0x1204	RW	2	IPI_Enalbe
Core2_IPI_Set	0x1208	W	2	IPI_Set
Core2_IPI_Clear	0x120c	W	2	IPI_Clear
Core2_MailBox0	0x1220	R	2	IPI_MailBox0
Core2_MailBox1	0x1228	RW	2	IPI_MailBox1
Core2_MailBox2	0x1230	W	2	IPI_MailBox2
Core2_MailBox3	0x1238	W	2	IPI_MailBox3

10- 5 3

Core3_IPI_Status	0x1300	R	3	IPI_Status
Core3_IPI_Enalbe	0x1304	RW	3	IPI_Enalbe
Core3_IPI_Set	0x1308	W	3	IPI_Set
Core3_IPI_Clear	0x130c	W	3	IPI_Clear

Core3_MailBox0	0x1320	R	3	IPI_MailBox0
Core3_MailBox1	0x1328	RW	3	IPI_MailBox1
Core3_MailBox2	0x1330	W	3	IPI_MailBox2
Core3_MailBox3	0x1338	W	3	IPI_MailBox3

10- 6

perCore_IPI_Status	0x1000	R	IPI_Status
perCore_IPI_Enalbe	0x1004	RW	IPI_Enalbe
perCore_IPI_Set	0x1008	W	IPI_Set
perCore_IPI_Clear	0x100c	W	IPI_Clear
perCore_MailBox0	0x1020	RW	IPI_MailBox0
perCore_MailBox1	0x1028	RW	IPI_MailBox1
perCore_MailBox2	0x1030	RW	IPI_MailBox2
perCore_MailBox3	0x1038	RW	IPI_MailBox3

10- 7

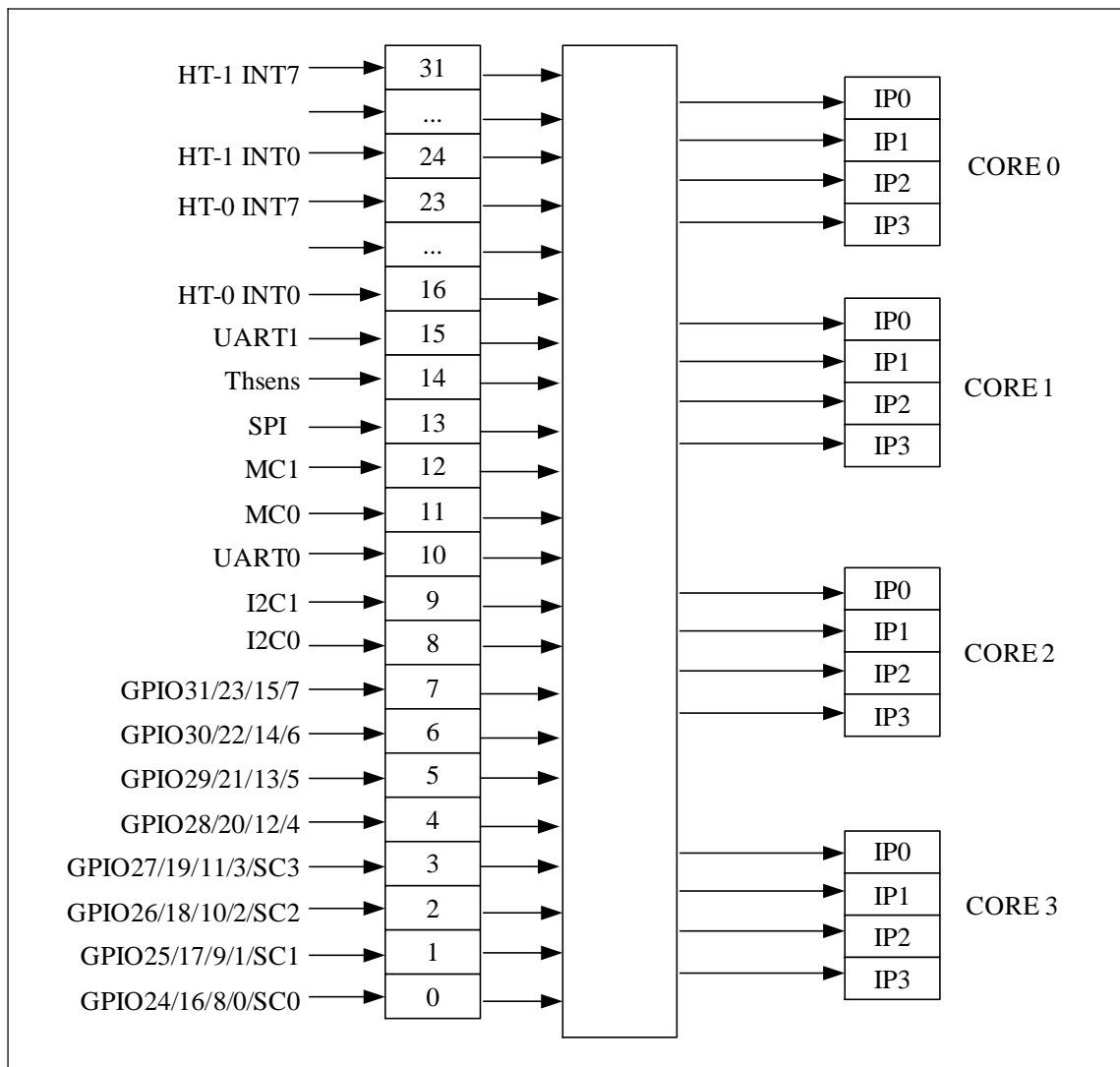
IPI_Send	0x1040	WO	32 [31] [30:26] [25:16] [15:5] [4:0]	1 IPI_Status
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Mail_Send	0x1048	WO	<p>64 MailBox</p> <p>[63:32] MailBox</p> <p>[31] 1</p> <p>[30:27] mask 32</p> <p>1000b</p> <p>0-2 0000b 0-3</p> <p>[26]</p> <p>[25:16]</p> <p>[15:5]</p> <p>[4:2] MailBox</p> <p>0 - MailBox0 32</p> <p>1 - MailBox0 32</p> <p>2 - MailBox1 32</p> <p>3 - MailBox1 32</p> <p>4 - MailBox2 32</p> <p>5 - MailBox2 32</p> <p>6 - MailBox3 32</p> <p>7 - MailBox4 32</p> <p>[1:0]</p>
FREQ_Send	0x1058	WO	<p>32</p> <p>[31] 1</p> <p>[30:27] mask 32</p> <p>1000b</p> <p>0-2 0000b 0-3</p> <p>[26]</p> <p>[25:16]</p> <p>[15:5]</p> <p>[4:0]</p> <p>CSR[0x1050]</p>

10- 8

ANY_Send	0x1158	WO	64
			[63:32]
			[31]
			[30:27]
			mask
			32
			1000b
			0-2
			0000b
			0-3
			[26]
			[25:16]
			[15:0]



11- 1 3C5000L

11- 1

	Intedge	Inten	Intenset	Intenclr	
0	RW / 0	R / 0	RW / 0	RW / 0	GPIO24/16/8/0/SC0
1	RW / 0	R / 0	RW / 0	RW / 0	GPIO25/17/9/1/SC1
2	RW / 0	R / 0	RW / 0	RW / 0	GPIO26/18/10/2/SC
					2
3					

11- 2 IO

Intisr	0x1420	32
Inten	0x1424	32
Intenset	0x1428	32
Intenclr	0x142c	32
Intedge	0x1434	32
CORE0_INTISR	0x1440	CORE0 32
CORE1_INTISR	0x1448	CORE1 32
CORE2_INTISR	0x1450	CORE2 32
CORE3_INTISR	0x1458	CORE3 32

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11- 3

3:0	
7:4	

11- 4

Entry0	0x1400	GPIO24/16/8/0	Entry16	0x1410	HT0-int0

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Entry1	0x1401	GPIO25/17/9/1	Entry17	0x1411	HT0-int1
Entry2	0x1402	GPIO26/18/10/2	Entry18	0x1412	HT0-int2
Entry3	0x1403	GPIO27/19/11/3	Entry19	0x1413	HT0-int3
Entry4	0x1404	GPIO28/20/12/4	Entry20	0x1414	HT0-int4
Entry5	0x1405	GPIO29/21/13/5	Entry21	0x1415	HT0-int5
Entry6	0x1406	GPIO30/22/14/6	Entry22	0x1416	HT0-int6
Entry7	0x1407	GPIO31/23/15/7	Entry23	0x1417	HT0-int7
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MC0	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11- 5

perCore_INTISR	0x1010	32

11- 6

48	EXT_INT_en	RW	OxO	IO
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11- 7 IO

EXT_IOLen[63:0]	0x1600	IO	[63:0]
EXT_IOLen[127:64]	0x1608	IO	[127:64]
EXT_IOLen[191:128]	0x1610	IO	[191:128]
EXT_IOLen[255:192]	0x1618	IO	[255:192]

11- 8 IO

EXT_IOIbounce[63:0]	0x1680	IO	[63:0]
EXT_IOIbounce[127:64]	0x1688	IO	[127:64]
EXT_IOIbounce[191:128]	0x1690	IO	[191:128]
EXT_IOIbounce[255:192]	0x1698	IO	[255:192]

11- 9 IO

EXT_IOLsr[63:0]	0x1700	IO	[63:0]
EXT_IOLsr[127:64]	0x1708	IO	[127:64]
EXT_IOLsr[191:128]	0x1710	IO	[191:128]
EXT_IOLsr[255:192]	0x1718	IO	[255:192]

11- 10		IO		
CORE0_EXT_IOLsr[63:0]	0x1800	0	IO	[63:0]
CORE0_EXT_IOLsr[127:64]	0x1808	0	IO	[127:64]
CORE0_EXT_IOLsr[191:128]	0x1810	0	IO	[191:128]
CORE0_EXT_IOLsr[255:192]	0x1818	0	IO	[255:192]
CORE1_EXT_IOLsr[63:0]	0x1900	1	IO	[63:0]
CORE1_EXT_IOLsr[127:64]	0x1908	1	IO	[127:64]
CORE1_EXT_IOLsr[191:128]	0x1910	1	IO	[191:128]
CORE1_EXT_IOLsr[255:192]	0x1918	1	IO	[255:192]
CORE2_EXT_IOLsr[63:0]	0x1A00	2	IO	[63:0]
CORE2_EXT_IOLsr[127:64]	0x1A08	2	IO	[127:64]
CORE2_EXT_IOLsr[191:128]	0x1A10	2	IO	[191:128]
CORE2_EXT_IOLsr[255:192]	0x1A18	2	IO	[255:192]
CORE3_EXT_IOLsr[63:0]	0x1B00	3	IO	[63:0]
CORE3_EXT_IOLsr[127:64]	0x1B08	3	IO	[127:64]
CORE3_EXT_IOLsr[191:128]				



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EXT_IOlmap_Core255	0x1CFF	EXT_IOI[255]
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11- 15

EXT_IOI_node_type0	0x14A0	16	0
EXT_IOI_node_type1	0x14A2	16	1
EXT_IOI_node_type2	0x14A4	16	2
.....			
EXT_IOI_node_type15	0x14BE	16	15

11- 16

IO



perCore_EXT_IOIsr[63:0]

0x1800

IO



12- 1

24	Thsens0_overflow	R		0
25	Thsens1_overflow	R		1
47:32	Thsens0_out	R		0 $=Thsens0_out * 731 / 0x4000$ $- 273$ $-40 \quad - 125$
65:48	Thsens1_out	R		1 $=Thsens1_out$ $-* 731 / 0x4000 - 273$ $-40 \quad - 125$

12- 2 IO

Thsens_Temperature	0x0428	R	



12- 3



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12- 4

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11:9	Temp_cluster	RW	0	Thsens_trigger
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=data*731/0x4000-273 -40 ~ 125

12- 7

Cluster	
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13- 1 DDR4 SDRAM

13- 2

13- 2 DDR4 SDRAM

13- 1

Offset	63:55	55:48	47:40	39:32	31:24	23:16	15:8	7:0
PHY								
0x0000							version(RD)	
0x0008			x4_mode	ddr3_mode			capability RD	
0x0010							dram_init(RD)	init_start
0x0018								
0x0020							preamble2	rdfifo_valid

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0x0028		rdfifo_empty(RD)				Overflow(RD)		
0x0030		dll_value(RD)	dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adj_cnt	dll_increment	dll_start_point
0x0038				dll_dbl_fix			dll_close_disable	dll_ck
0x0040				dbl_ctrl_ckca				dll_dbl_ckca
0x0048	pll_ctrl_ckca				pll_lock_ckca(RD)	dll_lock_ckca(RD)	clken_ckca	cksel_ckca
0x0050				dbl_ctrl_ds_0				dll_dbl_ds_0
0x0058	pll_ctrl_ds_0				pll_lock_ds_0(RD)	dll_lock_ds_0(RD)	clken_ds_0	cksel_ds_0
0x0060				dbl_ctrl_ds_1				dll_dbl_ds_1
0x0068	pll_ctrl_ds_1				pll_lock_ds_1(RD)	dll_lock_ds_1(RD)	clken_ds_1	cksel_ds_1
0x0070				dbl_ctrl_ds_2				dll_dbl_ds_2
0x0078	pll_ctrl_ds_2				pll_lock_ds_2(RD)	dll_lock_ds_2(RD)	clken_ds_2	cksel_ds_2
0x0080				dbl_ctrl_ds_3				dll_dbl_ds_3
0x0088	pll_ctrl_ds_3				pll_lock_ds_3(RD)	dll_lock_ds_3(RD)	clken_ds_3	cksel_ds_3
0x0090				dbl_ctrl_ds_4				dll_dbl_ds_4
0x0098	pll_ctrl_ds_4				pll_lock_ds_4(RD)	dll_lock_ds_4(RD)	clken_ds_4	cksel_ds_4
0x00a0				dbl_ctrl_ds_5				dll_dbl_ds_5
0x00a8	pll_ctrl_ds_5				pll_lock_ds_5(RD)	dll_lock_ds_5(RD)	clken_ds_5	cksel_ds_5
0x00b0				dbl_ctrl_ds_6				dll_dbl_ds_6
0x00b8	pll_ctrl_ds_6				pll_lock_ds_6(RD)	dll_lock_ds_6(RD)	clken_ds_6	cksel_ds_6
0x00c0				dbl_ctrl_ds_7				dll_dbl_ds_7
0x00c8	pll_ctrl_ds_7				pll_lock_ds_7(RD)	dll_lock_ds_7(RD)	clken_ds_7	cksel_ds_7
0x00d0				dbl_ctrl_ds_8				dll_dbl_ds_8
0x00d8	pll_ctrl_ds_8				pll_lock_ds_8(RD)	dll_lock_ds_8(RD)	clken_ds_8	cksel_ds_8
0x00e0			vrefclk_inv	vref_sample		vref_num	vref_dly	dll_vref
0x0100					dll_1xdly_0	dll_1xgen_0	dll_wrddqs_0	dll_wrddq_0
0x0108						dll_gate_0	dll_rddqs1_0	dll_rddqs0_0
0x0110	rdodt_ctrl_0	rdgate_len_0	rdgate_mode_0	rdgate_ctrl_0			cdqs_oe_ctrl_0	dq_oe_ctrl_0
0x0118						dly_2x_0	redge_sel_0	rddqs_phase_0(RD)
0x0120	w_bdlly0_0[31:28]	w_bdlly0_0[27:24]	w_bdlly0_0[23:20]	w_bdlly0_0[19:16]	w_bdlly0_0[15:12]	w_bdlly0_0[11:8]	w_bdlly0_0[7:4]	w_bdlly0_0[3:0]
0x0128		w_bdlly0_0[59:56]	w_bdlly0_0[55:52]	w_bdlly0_0[51:48]	w_bdlly0_0[47:44]	w_bdlly0_0[43:40]	w_bdlly0_0[39:36]	w_bdlly0_0[35:32]
0x0130	w_bdlly1_0[24:21]	w_bdlly1_0[20:18]	w_bdlly1_0[17:15]	w_bdlly1_0[14:12]	w_bdlly1_0[11:9]	w_bdlly1_0[8:6]	w_bdlly1_0[5:3]	w_bdlly1_0[2:0]
0x0138								w_bdlly1_0[27:26]
0x0140							rg_bdlly_0[7:4]	rg_bdlly_0[3:0]
0x0148								
0x0150	rdqsp_bdlly_0[31:28]	rdqsp_bdlly_0[27:24]	rdqsp_bdlly_0[23:20]	rdqsp_bdlly_0[19:16]	rdqsp_bdlly_0[15:12]	rdqsp_bdlly_0[11:8]	rdqsp_bdlly_0[7:4]	rdqsp_bdlly_0[3:0]
0x0158								rdqsp_bdlly_0[35:32]
0x0160	rdqsn_bdlly_0[31:28]	rdqsn_bdlly_0[27:24]	rdqsn_bdlly_0[23:20]	rdqsn_bdlly_0[19:16]	rdqsn_bdlly_0[15:12]	rdqsn_bdlly_0[11:8]	rdqsn_bdlly_0[7:4]	rdqsn_bdlly_0[3:0]

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0x0168								rdqsn_bdy_0[35:32]
0x0170	rdq_bdy_0[24:21]	rdq_bdy_0[20:18]	rdq_bdy_0[17:15]	rdq_bdy_0[14:12]	rdq_bdy_0[11:9]	rdq_bdy_0[8:6]	rdq_bdy_0[5:3]	rdq_bdy_0[2:0]
0x0178								rdq_bdy_0[27:26]
0x0180					dll_1xdly_1	dll_1xgen_1	dll_wrqqs_1	dll_wrdq_1
0x0188						dll_gate_1	dll_rddqs1_1	dll_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1	rdgate_ctrl_1			dqs_oe_ctrl_1	dq_oe_ctrl_1
0x0198						dly_2x_1	redge_sel_1	rddqs_phase_1(RD)
0x01a0	w_bdy0_1[31:28]	w_bdy0_1[27:24]	w_bdy0_1[23:20]	w_bdy0_1[19:16]	w_bdy0_1[15:12]	w_bdy0_1[11:8]	w_bdy0_1[7:4]	w_bdy0_1[3:0]
0x01a8		w_bdy0_1[59:56]	w_bdy0_1[55:52]	w_bdy0_1[51:48]	w_bdy0_1[47:44]	w_bdy0_1[43:40]	w_bdy0_1[39:36]	w_bdy0_1[35:32]
0x01b0	w_bdy1_1[24:21]	w_bdy1_1[20:18]	w_bdy1_1[17:15]	w_bdy1_1[14:12]	w_bdy1_1[11:9]	w_bdy1_1[8:6]	w_bdy1_1[5:3]	w_bdy1_1[2:0]
0x01b8								w_bdy1_1[27:26]
0x01c0							rg_bdy_1[7:4]	rg_bdy_1[3:0]
0x01c8								
0x01d0	rdqsp_bdy_1[31:28]	rdqsp_bdy_1[27:24]	rdqsp_bdy_1[23:20]	rdqsp_bdy_1[19:16]	rdqsp_bdy_1[15:12]	rdqsp_bdy_1[11:8]	rdqsp_bdy_1[7:4]	rdqsp_bdy_1[3:0]
0x01d8								rdqsp_bdy_1[35:32]
0x01e0	rdqsn_bdy_1[31:28]	rdqsn_bdy_1[27:24]	rdqsn_bdy_1[23:20]	rdqsn_bdy_1[19:16]	rdqsn_bdy_1[15:12]	rdqsn_bdy_1[11:8]	rdqsn_bdy_1[7:4]	rdqsn_bdy_1[3:0]
0x01e8								rdqsn_bdy_1[35:32]
0x01f0	rdq_bdy_1[24:21]	rdq_bdy_1[20:18]	rdq_bdy_1[17:15]	rdq_bdy_1[14:12]	rdq_bdy_1[11:9]	rdq_bdy_1[8:6]	rdq_bdy_1[5:3]	rdq_bdy_1[2:0]
0x01f8								rdq_bdy_1[27:26]
0x0200					dll_1xdly_2	dll_1xgen_2	dll_wrqqs_2	dll_wrdq_2
0x0208						dll_gate_2	dll_rddqs1_2	dll_rddqs0_2
0x0210	rdodt_ctrl_2	rdgate_len_2	rdgate_mode_2	rdgate_ctrl_2			dqs_oe_ctrl_2	dq_oe_ctrl_2
0x0218						dly_2x_2	redge_sel_2	rddqs_phase_2(RD)
0x0220	w_bdy0_2[31:28]	w_bdy0_2[27:24]	w_bdy0_2[23:20]	w_bdy0_2[19:16]	w_bdy0_2[15:12]	w_bdy0_2[11:8]	w_bdy0_2[7:4]	w_bdy0_2[3:0]
0x0228		w_bdy0_2[59:56]	w_bdy0_2[55:52]	w_bdy0_2[51:48]	w_bdy0_2[47:44]	w_bdy0_2[43:40]	w_bdy0_2[39:36]	w_bdy0_2[35:32]
0x0230	w_bdy1_2[24:21]	w_bdy1_2[20:18]	w_bdy1_2[17:15]	w_bdy1_2[14:12]	w_bdy1_2[11:9]	w_bdy1_2[8:6]	w_bdy1_2[5:3]	w_bdy1_2[2:0]
0x0238								w_bdy1_2[27:26]
0x0240							rg_bdy_2[7:4]	rg_bdy_2[3:0]
0x0248								
0x0250	rdqsp_bdy_2[31:28]	rdqsp_bdy_2[27:24]	rdqsp_bdy_2[23:20]	rdqsp_bdy_2[19:16]	rdqsp_bdy_2[15:12]	rdqsp_bdy_2[11:8]	rdqsp_bdy_2[7:4]	rdqsp_bdy_2[3:0]
0x0258								rdqsp_bdy_2[35:32]
0x0260	rdqsn_bdy_2[31:28]	rdqsn_bdy_2[27:24]	rdqsn_bdy_2[23:20]	rdqsn_bdy_2[19:16]	rdqsn_bdy_2[15:12]	rdqsn_bdy_2[11:8]	rdqsn_bdy_2[7:4]	rdqsn_bdy_2[3:0]
0x0268								rdqsn_bdy_2[35:32]
0x0270	rdq_bdy_2[24:21]	rdq_bdy_2[20:18]	rdq_bdy_2[17:15]	rdq_bdy_2[14:12]	rdq_bdy_2[11:9]	rdq_bdy_2[8:6]	rdq_bdy_2[5:3]	rdq_bdy_2[2:0]
0x0278								rdq_bdy_2[27:26]
0x0280					dll_1xdly_3	dll_1xgen_3	dll_wrqqs_3	dll_wrdq_3

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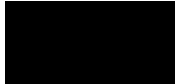
0x0288						dll_gate_3	dll_rddqs1_3	dll_rddqs0_3
0x0290	rdodt_ctrl_3	rdgate_len_3	rdgate_mode_3	rdgate_ctrl_3			dqs_oe_ctrl_3	dq_oe_ctrl_3
0x0298						dly_2x_3	redge_sel_3	rddqs_phase_3(RD)
0x02a0	w_bdy0_3[31:28]	w_bdy0_3[27:24]	w_bdy0_3[23:20]	w_bdy0_3[19:16]	w_bdy0_3[15:12]	w_bdy0_3[11:8]	w_bdy0_3[7:4]	w_bdy0_3[3:0]
0x02a8		w_bdy0_3[59:56]	w_bdy0_3[55:52]	w_bdy0_3[51:48]	w_bdy0_3[47:44]	w_bdy0_3[43:40]	w_bdy0_3[39:36]	w_bdy0_3[35:32]
0x02b0	w_bdy1_3[24:21]	w_bdy1_3[20:18]	w_bdy1_3[17:15]	w_bdy1_3[14:12]	w_bdy1_3[11:9]	w_bdy1_3[8:6]	w_bdy1_3[5:3]	w_bdy1_3[2:0]
0x02b8								w_bdy1_3[27:26]
0x02c0							rg_bdy_3[7:4]	rg_bdy_3[3:0]
0x02c8								
0x02d0	rdqsp_bdy_3[31:28]	rdqsp_bdy_3[27:24]	rdqsp_bdy_3[23:20]	rdqsp_bdy_3[19:16]	rdqsp_bdy_3[15:12]	rdqsp_bdy_3[11:8]	rdqsp_bdy_3[7:4]	rdqsp_bdy_3[3:0]
0x02d8								rdqsp_bdy_3[35:32]
0x02e0	rdqsn_bdy_3[31:28]	rdqsn_bdy_3[27:24]	rdqsn_bdy_3[23:20]	rdqsn_bdy_3[19:16]	rdqsn_bdy_3[15:12]	rdqsn_bdy_3[11:8]	rdqsn_bdy_3[7:4]	rdqsn_bdy_3[3:0]
0x02e8								rdqsn_bdy_3[35:32]
0x02f0	rdq_bdy_3[24:21]	rdq_bdy_3[20:18]	rdq_bdy_3[17:15]	rdq_bdy_3[14:12]	rdq_bdy_3[11:9]	rdq_bdy_3[8:6]	rdq_bdy_3[5:3]	rdq_bdy_3[2:0]
0x02f8								rdq_bdy_3[27:26]
0x0300					dll_1xgdy_4	dll_1xgen_4	dll_wrqqs_4	dll_wrdq_4
0x0308						dll_gate_4	dll_rddqs1_4	dll_rddqs0_4
0x0310	rdodt_ctrl_4	rdgate_len_4	rdgate_mode_4	rdgate_ctrl_4			dqs_oe_ctrl_4	dq_oe_ctrl_4
0x0318						dly_2x_4	redge_sel_4	rddqs_phase_4(RD)
0x0320	w_bdy0_4[31:28]	w_bdy0_4[27:24]	w_bdy0_4[23:20]	w_bdy0_4[19:16]	w_bdy0_4[15:12]	w_bdy0_4[11:8]	w_bdy0_4[7:4]	w_bdy0_4[3:0]
0x0328		w_bdy0_4[59:56]	w_bdy0_4[55:52]	w_bdy0_4[51:48]	w_bdy0_4[47:44]	w_bdy0_4[43:40]	w_bdy0_4[39:36]	w_bdy0_4[35:32]
0x0330	w_bdy1_4[24:21]	w_bdy1_4[20:18]	w_bdy1_4[17:15]	w_bdy1_4[14:12]	w_bdy1_4[11:9]	w_bdy1_4[8:6]	w_bdy1_4[5:3]	w_bdy1_4[2:0]
0x0338								w_bdy1_4[27:26]
0x0340							rg_bdy_4[7:4]	rg_bdy_4[3:0]
0x0348								
0x0350	rdqsp_bdy_4[31:28]	rdqsp_bdy_4[27:24]	rdqsp_bdy_4[23:20]	rdqsp_bdy_4[19:16]	rdqsp_bdy_4[15:12]	rdqsp_bdy_4[11:8]	rdqsp_bdy_4[7:4]	rdqsp_bdy_4[3:0]
0x0358								rdqsp_bdy_4[35:32]
0x0360	rdqsn_bdy_4[31:28]	rdqsn_bdy_4[27:24]	rdqsn_bdy_4[23:20]	rdqsn_bdy_4[19:16]	rdqsn_bdy_4[15:12]	rdqsn_bdy_4[11:8]	rdqsn_bdy_4[7:4]	rdqsn_bdy_4[3:0]
0x0368								rdqsn_bdy_4[35:32]
0x0370	rdq_bdy_4[24:21]	rdq_bdy_4[20:18]	rdq_bdy_4[17:15]	rdq_bdy_4[14:12]	rdq_bdy_4[11:9]	rdq_bdy_4[8:6]	rdq_bdy_4[5:3]	rdq_bdy_4[2:0]
0x0378								rdq_bdy_4[27:26]
0x0380					dll_1xgdy_5	dll_1xgen_5	dll_wrqqs_5	dll_wrdq_5
0x0388						dll_gate_5	dll_rddqs1_5	dll_rddqs0_5
0x0390	rdodt_ctrl_5	rdgate_len_5	rdgate_mode_5	rdgate_ctrl_5			dqs_oe_ctrl_5	dq_oe_ctrl_5
0x0398						dly_2x_5	redge_sel_5	rddqs_phase_5(RD)
0x03a0	w_bdy0_5[31:28]	w_bdy0_5[27:24]	w_bdy0_5[23:20]	w_bdy0_5[19:16]	w_bdy0_5[15:12]	w_bdy0_5[11:8]	w_bdy0_5[7:4]	w_bdy0_5[3:0]



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0x03a8	w_bdy0_5[59:56]	w_bdy0_5[55:52]	w_bdy0_5[51:48]	w_bdy0_5[47:44]	w_bdy0_5[43:40]	w_bdy0_5[39:36]	w_bdy0_5[35:32]
0x03b0	w_bdy1_5[24:21]	w_bdy1_5[20:18]	w_bdy1_5[17:15]	w_bdy1_5[14:12]	w_bdy1_5[11:9]	w_bdy1_5[8:6]	w_bdy1_5[5:3]
0x03b8							w_bdy1_5[27:26]
0x03c0						rg_bdy_5[7:4]	rg_bdy_5[3:0]
0x03c8							
0x03d0	rdqsp_bdy_5[31:28]	rdqsp_bdy_5[27:24]	rdqsp_bdy_5[23:20]	rdqsp_bdy_5[19:16]	rdqsp_bdy_5[15:12]	rdqsp_bdy_5[11:8]	rdqsp_bdy_5[7:4]
0x03d8							

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0x04c8									
0x04d0	rdqsp_bdly_7[31:28]	rdqsp_bdly_7[27:24]	rdqsp_bdly_7[23:20]	rdqsp_bdly_7[19:16]	rdqsp_bdly_7[15:12]	rdqsp_bdly_7[11:8]	rdqsp_bdly_7[7:4]	rdqsp_bdly_7[3:0]	
0x04d8								rdqsp_bdly_7[35:32]	
0x04e0	rdqsn_bdly_7[31:28]	rdqsn_bdly_7[27:24]	rdqsn_bdly_7[23:20]	rdqsn_bdly_7[19:16]	rdqsn_bdly_7[15:12]	rdqsn_bdly_7[11:8]	rdqsn_bdly_7[7:4]	rdqsn_bdly_7[3:0]	
0x04e8								rdqsn_bdly_7[35:32]	
0x04f0	rdq_bdly_7[24:21]	rdq_bdly_7[20:18]	rdq_bdly_7[17:15]	rdq_bdly_7[14:12]	rdq_bdly_7[11:9]	rdq_bdly_7[8:6]	rdq_bdly_7[5:3]	rdq_bdly_7[2:0]	
0x04f8								rdq_bdly_7[27:26]	
0x0500					dll_1xcdly_8	dll_1xgen_8	dll_wrqqs_8	dll_wrdq_8	
0x0508						dll_gate_8	dll_rddqs1_8	dll_rddqs0_8	
0x0510	rdodt_ctrl_8	rdgate_len_8	rdgate_mode_8	rdgate_ctrl_8			dqs_oe_ctrl_8	dq_oe_ctrl_8	
0x0518						dly_2x_8	redge_sel_8	rddqs_phase_8(RD)	
0x0520	w_bdly0_8[31:28]	w_bdly0_8[27:24]	w_bdly0_8[23:20]	w_bdly0_8[19:16]	w_bdly0_8[15:12]	w_bdly0_8[11:8]	w_bdly0_8[7:4]	w_bdly0_8[3:0]	
0x0528		w_bdly0_8[59:56]	w_bdly0_8[55:52]	w_bdly0_8[51:48]	w_bdly0_8[47:44]	w_bdly0_8[43:40]	w_bdly0_8[39:36]	w_bdly0_8[35:32]	
0x0530	w_bdly1_8[24:21]	w_bdly1_8[20:18]	w_bdly1_8[17:15]	w_bdly1_8[14:12]	w_bdly1_8[11:9]	w_bdly1_8[8:6]	w_bdly1_8[5:3]	w_bdly1_8[2:0]	
0x0538								w_bdly1_8[27:26]	
0x0540							rg_bdly_8[7:4]	rg_bdly_8[3:0]	
0x0548									
0x0550	rdqsp_bdly_8[31:28]	rdqsp_bdly_8[27:24]	rdqsp_bdly_8[23:20]	rdqsp_bdly_8[19:16]	rdqsp_bdly_8[15:12]	rdqsp_bdly_8[11:8]	rdqsp_bdly_8[7:4]	rdqsp_bdly_8[3:0]	
0x0558								rdqsp_bdly_8[35:32]	
0x0560	rdqsn_bdly_8[31:28]	rdqsn_bdly_8[27:24]	rdqsn_bdly_8[23:20]	rdqsn_bdly_8[19:16]	rdqsn_bdly_8[15:12]	rdqsn_bdly_8[11:8]	rdqsn_bdly_8[7:4]	rdqsn_bdly_8[3:0]	
0x0568								rdqsn_bdly_8[35:32]	
0x0570	rdq_bdly_8[24:21]	rdq_bdly_8[20:18]	rdq_bdly_8[17:15]	rdq_bdly_8[14:12]	rdq_bdly_8[11:9]	rdq_bdly_8[8:6]	rdq_bdly_8[5:3]	rdq_bdly_8[2:0]	
0x0578								rdq_bdly_8[27:26]	
0x0700					leveling_cs	tLM_DELAY	leveling_req(WR)	leveling_mode	
0x0708							leveling_done(RD)	leveling_ready(RD)	
0x0710	leveling_resp_7	leveling_resp_6	leveling_resp_5	leveling_resp_4	leveling_resp_3	leveling_resp_2	leveling_resp_1	leveling_resp_0	
0x0718								leveling_resp_8	
0x0720									
0x0800	dfe_ctrl_ds	pad_ctrl_ds					pad_ctrl_ck		
0x0808		pad_reset_po	pad_oplen_ca	pad_opdly_ca		pad_ctrl_ca			
0x0810	vref_ctrl_ds_3		vref_ctrl_ds_2		vref_ctrl_ds_1		vref_ctrl_ds_0		
0x0818	vref_ctrl_ds_7		vref_ctrl_ds_6		vref_ctrl_ds_5		vref_ctrl_ds_4		
0x0820							vref_ctrl_ds_8		
0x0828									



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0x1188			mr_6_cs_0_ddr4		mr_5_cs_0_ddr4		mr_4_cs_0_ddr4	
0x1190	mr_3_cs_1_ddr4		mr_2_cs_1_ddr4		mr_1_cs_1_ddr4		mr_0_cs_1_ddr4	
0x1198			mr_6_cs_1_ddr4		mr_5_cs_1_ddr4		mr_4_cs_1_ddr4	
0x11a0	mr_3_cs_2_ddr4		mr_2_cs_2_ddr4		mr_1_cs_2_ddr4		mr_0_cs_2_ddr4	
0x11a8			mr_6_cs_2_ddr4		mr_5_cs_2_ddr4		mr_4_cs_2_ddr4	
0x11b0	mr_3_cs_3_ddr4		mr_2_cs_3_ddr4		mr_1_cs_3_ddr4		mr_0_cs_3_ddr4	
0x11b8			mr_6_cs_3_ddr4		mr_5_cs_3_ddr4		mr_4_cs_3_ddr4	
0x11c0	mr_3_cs_4_ddr4		mr_2_cs_4_ddr4		mr_1_cs_4_ddr4		mr_0_cs_4_ddr4	
0x11c8			mr_6_cs_4_ddr4		mr_5_cs_4_ddr4		mr_4_cs_4_ddr4	
0x11d0	mr_3_cs_5_ddr4		mr_2_cs_5_ddr4		mr_1_cs_5_ddr4		mr_0_cs_5_ddr4	
0x11d8			mr_6_cs_5_ddr4		mr_5_cs_5_ddr4		mr_4_cs_5_ddr4	
0x11e0	mr_3_cs_6_ddr4		mr_2_cs_6_ddr4		mr_1_cs_6_ddr4		mr_0_cs_6_ddr4	
0x11e8			mr_6_cs_6_ddr4		mr_5_cs_6_ddr4		mr_4_cs_6_ddr4	
0x11f0	mr_3_cs_7_ddr4		mr_2_cs_7_ddr4		mr_1_cs_7_ddr4		mr_0_cs_7_ddr4	
0x11f8			mr_6_cs_7_ddr4		mr_5_cs_7_ddr4		mr_4_cs_7_ddr4	
0x1200			nc16_map	nc	channel_width	ba_xor_row_offset	addr_new	cs_place
0x1208						bg_xor_row_offset		addr_mirror
0x1210	addr_base_1				addr_base_0			
0x1218								
0x1220	addr_mask_1				addr_mask_0			
0x1228								
0x1230			cs_diff	c_diff	bg_diff	ba_diff	row_diff	col_diff
0x1238				CF_confbus_timeout				
0x1240	WRQthreshold	tRDQidle	wr_pkc_num	rwq_rb	retry	no_dead_inorder	placement_en	stb_en/pbuf
0x1248								tRWGNIdle
0x1250							rfifo_age	
0x1258	prior_age3		prior_age2		prior_age1		prior_age0	
0x1260	retry_cnt(RD)					rbuffer_max(RD)	rdfifo_depth	stat_en
0x1268								
0x1270								
0x1280	aw_512_align		rd_before_wr	ecc_enable		int_vector(RD)	int_trigger(RD)	int_enable
0x1288								
0x1290						int_cnt_fatal(RD)	int_cnt_em(RD)	int_cnt
0x1298	ecc_cnt_cs_7(RD)	ecc_cnt_cs_6(RD)	ecc_cnt_cs_5(RD)	ecc_cnt_cs_4(RD)	ecc_cnt_cs_3(RD)	ecc_cnt_cs_2(RD)	ecc_cnt_cs_1(RD)	ecc_cnt_cs_0(RD)
0x12a0	ecc_data_dir(RD)	ecc_code_dir(RD)	ecc_code_256(RD)					ecc_code_64(RD)
0x12a8	ecc_addr(RD)							
0x12b0	ecc_data[63:0](RD)							
0x12b8	ecc_data[127:64] (RD)							
0x12c0	ecc_data[191:128] (RD)							
0x12c8	ecc_data[255:192] (RD)							

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0x1300							ref_num	ref_sch_en
0x1308							Status_sref(RD)	srefresh_req
0x1340	hardware_pd_7	hardware_pd_6	hardware_pd_5	hardware_pd_4	hardware_pd_3	hardware_pd_2	hardware_pd_1	hardware_pd_0
0x1348	power_sta_7(RD)	power_sta_6(RD)	power_sta_5(RD)	power_sta_4(RD)	power_sta_3(RD)	power_sta_2(RD)	power_sta_1(RD)	power_sta_0(RD)
0x1350	selfref_age		slowpd_age		fastpd_age		active_age	
0x1358				power_up				Age_step
0x1360	tCONF_IDLE				tLPMC_IDLE			
0x1380								zq_overlap
0x1388								zq_stat_en
0x1390	zq_cnt_1(RD)				zq_cnt_0(RD)			
0x1398	zq_cnt_3(RD)				zq_cnt_2(RD)			
0x13a0	zq_cnt_5(RD)				zq_cnt_4(RD)			
0x13a8	zq_cnt_6(RD)				zq_cnt_6(RD)			
0x13c0					odt_wr_cs_map			
0x13c8							odt_wr_length	odt_wr_delay
0x13d0					odt_rd_cs_map			
0x13d8							odt_rd_length	odt_rd_delay
0x1400				tRESYNC_length	tRESYNC_delay	tRESYNC_shift	tRESYNC_max	tRESYNC_min
0x1440					pre_predict		tm_cmdq_num	burst_length
0x1448								ca_timing
0x1450						wr/rd_dbi_en	ca_par_en	crc_en
0x1458							tCA_PAR	tWR_CRC
0x1460	bit_map_7	bit_map_6	bit_map_5	bit_map_6	bit_map_3	bit_map_2	bit_map_1	bit_map_0
0x1468	bit_map_15	bit_map_14	bit_map_13	bit_map_12	bit_map_11	bit_map_10	bit_map_9	bit_map_8
0x1470							bit_map_17	bit_map_16
0x1478								bitmap_mirror
0x1480				alern_misc(RD)			alern_cnt	alern_clr
0x1488	alern_addr(RD)							
0x1500	win0_base							
0x1508	win1_base							
0x1510	win2_base							
0x1518	win3_base							
0x1520	win4_base							

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0x1528	win5_base							
0x1530	win6_base							
0x1538	win7_base							
0x1580	win0_mask							
0x1588	win1_mask							
0x1590	win2_mask							
0x1598	win3_mask							
0x15a0	win4_mask							
0x15a8	win5_mask							
0x15b0	win6_mask							
0x15b8	win7_mask							
0x1600	win0_mmap							
0x1608	win1_mmap							
0x1610	win2_mmap							
0x1618	win3_mmap							
0x1620	win4_mmap							
0x1628	win5_mmap							
0x1630	win6_mmap							
0x1638	win7_mmap							
0x1700							acc_hp	acc_en
0x1708	acc_fake_b				acc_fake_a			
0x1710								
0x1718								
0x1720	addr_base_acc_1				addr_base_acc_0			
0x1728								
0x1730	addr_mask_acc_1				addr_mask_acc_0			
0x1738								
MON								
0x2000								cmd_monitor
0x2008								
0x2010	cmd_fbck[63:0](RD)							
0x2018	cmd_fbck[127:64](RD)							
0x2020					rw_switch_cnt(RD)			
0x2100								scheduler_mon
0x2108								
0x2110	sch_cmd_num(RD)							

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0x2118	ba_conflict_all(RD)							
0x2120	ba_conflict_last1(RD)							
0x2128	ba_conflict_last2(RD)							
0x2130	ba_conflict_last3(RD)							
0x2138	ba_conflict_last4(RD)							
0x2140	ba_conflict_last5(RD)							
0x2148	ba_conflict_last6(RD)							
0x2150	ba_conflict_last7(RD)							
0x2158	ba_conflict_last8(RD)							
0x2160	rd_conflict(RD)							
0x2168	wr_conflict(RD)							
0x2170	rtw_conflict(RD)							
0x2178	wtr_conflict(RD)							
0x2180	rd_conflict_last1(RD)							
0x2188	wr_conflict_last1(RD)							
0x2190	rtw_conflict_last1(RD)							
0x2198	wtr_conflict_last1(RD)							
0x21a0	wr_rd_tumaround(RD)							
0x21a8	cs_tumaround(RD)							
0x21b0	bg_conflict(RD)							
0x2300						sm_leveling		sm_init
0x2308								
0x2310		sm_rank_03		sm_rank_02		sm_rank_01		sm_rank_00
0x2318		sm_rank_07		sm_rank_06		sm_rank_05		sm_rank_04
0x2320		sm_rank_11		sm_rank_10		sm_rank_09		sm_rank_08
0x2328		sm_rank_15		sm_rank_14		sm_rank_13		sm_rank_12
0x2330		sm_rank_19		sm_rank_18		sm_rank_17		sm_rank_16
0x2338		sm_rank_23		sm_rank_22		sm_rank_21		sm_rank_20
0x2340		sm_rank_27		sm_rank_26		sm_rank_25		sm_rank_24
0x2348		sm_rank_31		sm_rank_30		sm_rank_29		sm_rank_28
TST								
0x3000						lpbk_mode	lpbk_start	lpbk_en
0x3008	lpbk_correct(RD)				lpbk_counter(RD)			lpbk_error(RD)
0x3010	lpbk_data_en[63:0]							
0x3018								lpbk_data_en[71:64]
0x3020							lpbk_data_mask_en	
0x3028								
0x3030	lpbk_dat_w0[63:0]							

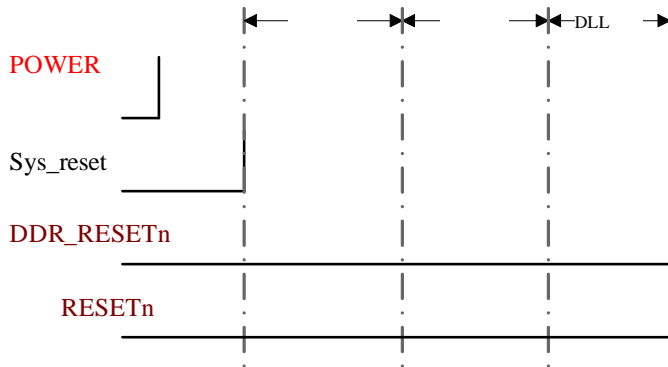
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0x3038	lpbk_dat_w0[127:64]							
0x3040	lpbk_dat_w1[63:0]							
0x3048	lpbk_dat_w1[127:64]							
0x3050		lpbk_ecc_mask_w 0	lpbk_dat_mask_w0				lpbk_ecc_w0	
0x3058		lpbk_ecc_mask_w 1	lpbk_dat_mask_w1				lpbk_ecc_w1	
0x3060								prbs_23
0x3068						prbs_init		
0x3100					fix_data_pattern_inde x	bus_width	page_size	test_engine_en
0x3108			cs_diff_tst	c_diff_tst	bg_diff_tst	ba_diff_tst	row_diff_tst	col_diff_tst
0x3120	addr_base_tst							
0x3128								
0x3130	user_data_pattern							
0x3138								
0x3140	valid_bits[63:0]							
0x3148								valid_bits[71:64]
0x3150	ctrl[63:0]							
0x3158	ctrl[127:64]							
0x3160	obs[63:0] (RD)							
0x3168	obs[127:64] (RD)							
0x3170	obs[191:128] (RD)							
0x3178	obs[255:192] (RD)							
0x3180	obs[319:256] (RD)							
0x3188	obs[383:320] (RD)							
0x3190	obs[447:384] (RD)							
0x3198	obs[511:448] (RD)							
0x31a0	obs[575:512] (RD)							
0x31a8	obs[639:576] (RD)							
0x31b0					obs[671:640](RD)			
0x3200								
0x3208								
0x3220	tud_i0							
0x3228	tud_i1							
0x3230	tud_o(RD)							
0x3300	tst_300							



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0x3308	tst_308
0x3310	tst_310
0x3318	tst_318
0x3320	tst_320
0x3328	tst_328
0x3330	tst_330
0x3338	tst_338
0x3340	tst_340
0x3348	tst_348
0x3350	tst_350
0x3358	tst_358
0x3360	tst_360
0x3368	tst_368
0x3370	tst_370
0x3378	tst_378

















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```
'      HT1.0/HT3.0
'      200/400/800/1600/2000/2400/3200MHz
'  HT1.0    8
'  HT3.0    8
'
'          PowerOK  Rstn  LDT_Stopn
'  DMA      Cache/Uncache
'
'          Cache
```

14- 1 HyperTransport

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HIO_8x2		1 16 HyperTransport 8 HIO_Lo address[40] = 0 HIO_Hi address[40] = 1; 1
HIO_Lo_mode		1 HIO_Lo HIO_Lo HIO_Lo_Powerok HIO_Lo_Rstn HIO_Lo_Ldt_Stopn "Act as Slave" 0 HyperTransport Bridge 1 0 0 HyperTransport P2P 1 0 HIO_Lo HIO_Lo_Powerok HIO_Lo_Rstn HIO_Lo_Ldt_Stopn HT
HIO_Lo_Powerok	Powerok	HyperTransport Powerok HIO_Lo_Mode 1 HIO_Lo HIO_Lo_Mode 0
HIO_Lo_Rstn	Rstn	HyperTransport Rstn HIO_Lo_Mode 1 HIO_Lo HIO_Lo_Mode 0
HIO_Lo_Ldt_Stopn	Ldt_Stopn	HyperTransport Ldt_Stopn HIO_Lo_Mode 1 HIO_Lo HIO_Lo_Mode 0
HIO_Lo_Ldt_Reqn	Ldt_Reqn	HyperTransport Ldt_Reqn
HIO_Hi_mode		
HIO_Hi_Powerok	Powerok	
HIO_Hi_Rstn	Rstn	
HIO_Hi_Ldt_Stopn	Ldt_Stopn	
HIO_Hi_Ldt_Reqn	Ldt_Reqn	
HIO_Rx_CLKp[1:0] HIO_Rx_CLKn[1:0] HIO_Tx_CLKp[1:0] HIO_Tx_CLKn[1:0]	CLK[1:0]	HyperTransport CLK
HIO_Rx_CILp[1:0] HIO_Rx_CILn[1:0] HIO_Tx_CILp[1:0] HIO_Tx_CILn[1:0]	CIL[1:0]	HyperTransport CIL

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HTO_Rx_CADp[15:0]	CAD[15:0]	HyperTransport CAD [15:8]
HTO_Rx_CADn[15:0]		
HTO_Tx_CADp[15:0]		
HTO_Tx_CADn[15:0]		

14- 2 HyperTransport

000000	-	NOP		
000001	NPC	FLUSH		
x01xxx	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care	bit 5 1 POSTED bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 1
01xxxx	NPC	Read	bit 3 Don't Care bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 Don't Care	bit 3 Don't Care bit 2 0 - Byte 1 - Doubleword bit 1 Don't Care bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	

111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111010	PC	Broadcast		
111011	NPC	RdAddr	----	
111100	PC	FENCE		
111111	-	Sync/Error	Sync/Error	

14- 3

000000	-	NOP		
x01x0x	NPC or PC	Write	bit 5 0- Nonposted 1 - Posted bit 2 0- Byte 1 - Doubleword bit 0 0	bit 5 1 POSTED bit 2 0- Byte 1 - Doubleword bit 0 1
010x0x	NPC	Read	bit 2 0- Byte 1 - Doubleword bit 0 Don't Care	bit 2 0- Byte 1 - Doubleword bit 0 1
110000	R	RdResponse		
110011	R	TgtDone		
110100	PC	WrCoherent	----	
110101	PC	WrAddr	----	
111000	R	RespCoherent	----	
111001	NPC	RdCoherent	----	
111011	NPC	RdAddr	----	
111111	-	Sync/Error		



14- 5 4 HyperTransport

0x0AC0_0000_0000	0x0AFF_FFFF_FFFF	1 Tbytes	HIO_LO
0x0B00_0000_0000	0x0BFF_FFFF_FFFF	1 Tbytes	HIO_HI
0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 Tbytes	HT1_LO
0x0F00_0000_0000	0x0FFF_FFFF_FFFF	1 Tbytes	HT1_HI

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14.5.10	3	HyperTransport	HyperTransport	act_as_slave 0 P2P HyperTransport act_as_slave 1
Post 14.5.12	2		HyperTransport Post Write	Post Write Post Write HyperTransport
14.5.13	2		Cache	IO HT HyperTransport HyperTransport
Uncache 14.5.14	2	HyperTransport	HyperTransport Uncache	3C5000L IO DMA Cache SCache IO Uncache IO

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21:0	Reserved	22	0x0		

14- 9 Command Capabilities Pointer Capability ID

31:29	Slave/Pri	3	0x0	R	Command HOST/Sec
28:26	Reserved	2	0x0	R	
25:21	Unit Count	5	0x0	R/W	Unit
20:16	Unit ID	5	0x0		
15:08	Capabilities Pointer	8	0x60	R	Cap
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

14- 10 Link Config Link Control

30:28	Link Width Out	3	0x0	R/W	HT Disconnect 000 8 001 16
27	Reserved	1	0x0		
26:24	Link Width In	3	0x0	R/W	HT Disconnect

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23	Dw Fc out	1	0x0	R	
22:20	Max Link Width out	3	0x1	R	HT 16bits
19	Dw Fc In	1	0x0	R	
18:16	Max Link Width In	3	0x1	R	HT 16bits
15:14	Reserved	2	0x0		
13	LDTSTOP# Tristate Enable	1	0x1	R/W	HT HT Disconnect HT PHY 1 0
12:10	Reserved	3	0x0		
9	CRC Error (hi)	1	0x0	R/W	8 CRC
8	CRC Error (lo)	1	0x0	R/W	8 CRC
7	Trans off	1	0x0	R/W	HT PHY 16 1 / 8 HT PHY 0 8 HT PHY 8 HT PHY bit 0
6	End of Chain	0	0x0	R	
5	Init Complete	1	0x0	R	HT
4	Link Fail	1	0x0	R	
3:2	Reserved	2	0x0		
1	CRC Flood Enable	1	0x0	R/W	CRC flood HT
0	Trans off (hi)	1	0x0	R/W	16 HT 8 8 PHY 1 8 HT PHY 0 8 HT PHY

14- 11 Revision ID Link Freq Link Error Link Freq Cap

31:16	Link Freq Cap	16	0x0000	R	HT PLL {3.2G,2.6G,2.4G,2.2G,2.0G,1.8G,1.6G, 1.4G,1.2G,1.0G,800M,600M,500M,400 M,300M,200M}

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15:14	Reserved	2	0x0		
13	Over Flow Error	1	0x0	R	HT
12	Protocol Error	1	0x0	R/W	
11:8	Link Freq	4	0x0	R/W	HT Disconnect Link Freq Cap PLL 0x1F4
7:0	Revision ID	8	0x60	R/W	

14- 12 Feature Capability

31:9	Reserved	23	0x0		
8	Extended Register	1	0x0	R	
7:4	Reserved	3	0x0		
3	Extended CIL Time	1	0x0	R	
2	CRC Test Mode	1	0x0	R	
1	LDISTOP#	1	0x1	R	LDISTOP#
0	Isochronous Mode	1	0x0	R	

14- 13 Error Retry

31:10	Reserved	22	0x0	R	


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9	Retry Count Rollover	1	0x0	R	Retry
8	Reserved	1	0x0	R	
7:6	Short Retry Attempts	2	0x0	R/W	Short Retry
5:1	Reserved	5	0x0	R	
0	Link Retry Enable	1	0x0	R/W	

14- 16 Interrupt Capability

Bit Range	Field Name	Width	Start	Access	Description
31:24	Capabilities Pointer	8	0x80	R	Interrupt discovery and configuration block
23:16	Index	8	0x0	R/W	
15:8	Capabilities Pointer	8	0x0	R	Capabilities Pointer
7:0	Capability ID	8	0x08	R	Hypertransport Capability ID

14- 17 Dataport

Bit Range	Field Name	Width	Start	Access	Description
31:0	Dataport	32	0x0	R/W	Index 0x10 0xa8 0xac

14- 18 IntrInfo 1

Bit Range	Field Name	Width	Start	Access	Description
31:24	IntrInfo[31:24]	8	0xF8	R	
23:2	IntrInfo[23:2]	22	0x0	R/W	IntrInfo[23:2] PIC IntrInfo
1:0	Reserved	2	0x0	R	

14- 19 IntrInfo 2

Bit Range	Field Name	Width	Start	Access	Description
31:0	IntrInfo[63:32]	32	0x0	R	



14- 20 HT 1

31:0	Interrupt_case [31:0]	32	0x0	R/W	HT [31:0] 0/HTHI 4

14- 21 HT 2

31:0	Interrupt_case [63:32]	32	0x0	R/W	HT [63:32] 0/HTHI 4

14- 22 HT 3

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31:0	Interrupt_case [95:64]	32	0x0	R/W	HT [95:64]	1 /HTHI 5

14- 23 HT 4

31:0	Interrupt_case [127:96]	32	0x0	R/W	HT [127:96]	1 /HTHI 5

14- 31 HT 5

31:0	Interrupt_case [159:128]	32	0x0	R/W	HT [159:128]	2 /HTHI 6

14- 24 HT 6

31:0	Interrupt_case [191:160]	32	0x0	R/W	HT [191:160]	2 /HTHI 6

14- 25 HT 7

31:0	Interrupt_case [223:192]	32	0x0	R/W	HT [223:192]	3 /HTHI 7



14- 27 HT

1

31:0	Interrupt_mask [31:0]	32	0x0	R/W	HT	[31:0] 0 /HTH 4

14- 28 HT

2

31:0	Interrupt_mask [63:32]	32	0x0	R/W	HT	[63:32] 0 /HTH 4

14- 29 HT

3

31:0	Interrupt_mask [95:64]	32	0x0	R/W	HT	[95:64] 1 /HTH 5

14- 30 HT

4

31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT	[127:96] 1 /HTH 5

14- 31 HT

5

31:0	Interrupt_mask [159:128]	32	0x0	R/W	HT [159:128] 2 /HTHI 6

14- 32 HT

6

31:0	Interrupt_mask [191:160]	32	0x0	R/W	HT [191:160] 2 /HTHI 6

14- 33 HT

7

31:0	Interrupt_mask [223:192]	32	0x0	R/W	HT [223:192] 3 /HTHI 7

14- 34 HT

8

31:0	Interrupt_mask [255:224]	32	0x0	R/W	HT [255:224] 3 /HTHI 7

14- 35 Link Train

31:23	Reserved	9	0x0	R			
22	21	Transmitter LS select	2	0x0	R/W	Disconnected	Inactive
						2'b00LS1	
						2'b01LS0	
						2'b10LS2	
						2'b11LS3	
14	Dsiable Cmd Throttling	1	0x0	R/W	HyperTransport 3.0 DWS	Non-info CMD	4
					1'b0	Cmd Throttling	
					1'b1	Cmd ~ -	

14- 36 HT

0

31	ht_rx_image0_en	1	0x0	R/W	HT	0	
30	ht_rx_image0_trans_en	1	0x0	R/W	HT	0	
29	ht_rx_image0_multi_node_en	1	0x0	R/W	HT	0	
						[39:37]	[46:44]
28	ht_rx_image0_conf_hit_en	1	0x0	R/W	HT	0	
						0	
25:0	ht_rx_image0_trans[49:24]	26	0x0	R/W	HT	0	[49:24]

14- 37 HT

0

31:16	ht_rx_image0_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

14- 38 HT

1

31	ht_rx_image1_en	1	0x0	R/W	HT	1	
30	ht_rx_image1_trans_en	1	0x0	R/W	HT	1	

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Offset	Register Name	Width	Reset	Access	Cache	Value	Field
29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT	1	[39:37] [46:44]
28	ht_rx_image1_conf_hit_en	1	0x0	R/W	HT	1	0
25:0	ht_rx_image1_trans[49:24]	26	0x0	R/W	HT	1	[49:24]

14- 39 HT

1

Offset	Register Name	Width	Reset	Access	Cache	Value	Field
31:16	ht_rx_image1_base[39:24]	16	0x0	R/W	HT	1	[39:24]
15:0	ht_rx_image1_mask[39:24]	16	0x0	R/W	HT	1	[39:24]

14- 40 HT

2

Offset	Register Name	Width	Reset	Access	Cache	Value	Field
31	ht_rx_image2_en	1	0x0	R/W	HT	2	
30	ht_rx_image2_trans_en	1	0x0	R/W	HT	2	
29	ht_rx_image2_multi_node_en	1	0x0	R/W	HT	2	[39:37] [46:44]
28	ht_rx_image2_conf_hit_en	1	0x0	R/W	HT	2	0
25:0	ht_rx_image2_trans[49:24]	26	0x0	R/W	HT	2	[49:24]

14- 41 HT

2

Offset	Register Name	Width	Reset	Access	Cache	Value	Field

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Offset	Register Name	Width	Reset	Access	Cache	Size	Range
31:16	ht_rx_image2_base[39:24]	16	0x0	R/W	HT	2	[39:24]
15:0	ht_rx_image2_mask[39:24]	16	0x0	R/W	HT	2	[39:24]

14- 42 HT

3

Offset	Register Name	Width	Reset	Access	Cache	Size	Range
31	ht_rx_image3_en	1	0x0	R/W	HT	3	
30	ht_rx_image3_trans_en	1	0x0	R/W	HT	3	
29	ht_rx_image3_multi_node_en	1	0x0	R/W	HT	3	[39:37] [46:44]
28	ht_rx_image3_conf_hit_en	1	0x0	R/W	HT	3	0
25:0	ht_rx_image3_trans[49:24]	26	0x0	R/W	HT	3	[49:24]

14- 43 HT

3

Offset	Register Name	Width	Reset	Access	Cache	Size	Range
31:16	ht_rx_image3_base[39:24]	16	0x0	R/W	HT	3	[39:24]
15:0	ht_rx_image3_mask[39:24]	16	0x0	R/W	HT	3	[39:24]

14- 44 HT

4

Offset	Register Name	Width	Reset	Access	Cache	Size	Range
31	ht_rx_image4_en	1	0x0	R/W	HT	4	
30	ht_rx_image4_trans_en	1	0x0	R/W	HT	4	

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Bit	Field Name	Width	Reset	Access	HT	Size	Address
29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT	4	[39:37] [46:44]
28	ht_rx_image4_conf_hit_en	1	0x0	R/W	HT	4	0
25:0	ht_rx_image4_trans[49:24]	26	0x0	R/W	HT	4	[49:24]

14- 45 HT

4

Bit	Field Name	Width	Reset	Access	HT	Size	Address
31:16	ht_rx_image4_base[39:24]	16	0x0	R/W	HT	4	[39:24]
15:0	ht_rx_image4_mask[39:24]	16	0x0	R/W	HT	4	[39:24]

14- 46

Bit	Field Name	Width	Reset	Access	HT	Size	Address
31	ht_rx_header_trans_ext	1	0x1	R/W			
30	ht_rx_header_trans_en	1	0x1	R/W			0xFD_FE000000 [39:24]
29:0	ht_rx_header_trans[53:24]	30	0xFE00	R/W			[53:25] [53:24]

14- 47

30	ht_rx_ext_header_trans_en	1	0x0	R/W	0xFE_00000000 [39:28]
29:0	ht_rx_ext_header_trans[53:24]	30	0x0	R/W	[53:24] [53:29]

14- 48 HT POST 0

31	ht_post0_en	1	0x0	R/W	HT	POST	0
30	ht_split0_en	1	0x0	R/W	HT	(CPU uncache ACC)	
29:23	Reserved	14	0x0				
15:0	ht_post0_trans[39:24]	16	0x0	R/W	HT	POST	0 [39:24]

14- 49 HT POST 0

31:16	ht_post0_base[39:24]	16	0x0	R/W	HT	POST	0 [39:24]

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15:0	ht_post0_mask[39:24]	16	0x0	R/W	HT	POST	0	[39:24]
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14- 50 HT POST 1

31	ht_post1_en	1	0x0	R/W	HT	POST	1	
30	ht_split1_en	1	0x0	R/W	HT	(CPU uncache ACC)		
29:16	Reserved	14	0x0					
15:0	ht_post1_trans[39:24]	16	0x0	R/W	HT	POST	1	[39:24]

14- 51 HT POST 1

31:16	ht_post1_base[39:24]	16	0x0	R/W	HT	POST	1	[39:24]
15:0	ht_post1_mask[39:24]	16	0x0	R/W	HT	POST	1	[39:24]

14- 52 HT 0

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31	ht_prefetch0_en	1	0x0	R/W	HT	0	
30:16	Reserved	15	0x0				
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT	0	[39:24]

14- 53 HT 0

31:16	ht_prefetch0_base[39:24]	16	0x0	R/W	HT	0	[39:24]
15:0	ht_prefetch0_mask[39:24]	16	0x0	R/W	HT	0	[39:24]

14- 54 HT 1

31	ht_prefetch1_en	1	0x0	R/W	HT	1	
30:16	Reserved	15	0x0				
15:0	ht_prefetch1_trans[39:24]	16	0x0	R/W	HT	1	[39:24]

14- 55 HT 1

31:16	ht_prefetch1_base[39:24]	16	0x0	R/W	HT	1	[39:24]
15:0	ht_prefetch1_mask[39:24]	16	0x0	R/W	HT	1	[39:24]



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30	ht_uncache1_trans_en	1	0x0	R/W	HT	uncache	1
29	ht_uncache1_multi_node_en	1	0x0	R/W	HT	uncache	1
28	ht_uncache1_conf_hit_en	1	0x0	R/W	HT	uncache	1
25:0	ht_uncache1_trans[49:24]	26	0x0	R/W	HT	uncache	1
					[49:24]		

14- 59 HT Uncache 1

31:16	ht_uncache1_base[39:24]	16	0x0	R/W	HT	uncache	1	[39:24]
15:0	ht_uncache1_mask[39:24]	16	0x0	R/W	HT	uncache	1	[39:24]

14- 60 HT Uncache 2

31	ht_uncache2_en	1	0x0	R/W	HT	uncache	2
30	ht_uncache2_trans_en	1	0x0	R/W	HT	uncache	2
29	ht_uncache2_multi_node_en	1	0x0	R/W	HT	uncache	2
28	ht_uncache2_24] ^a						



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		14- 61 HT	Uncache			2		
31:16	ht_uncache2_base[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]
15:0	ht_uncache2_mask[39:24]	16	0x0	R/W	HT	uncache	2	[39:24]

14- 64 HT P2P 0

31	ht_rx_p2p0_en	1	0x0	R/W	HT	P2P	0	
29:0	ht_rx_p2p0_trans[53:24]	30	0x0	R/W	HT	P2P	0	[53:24]

14- 65 HT P2P 0

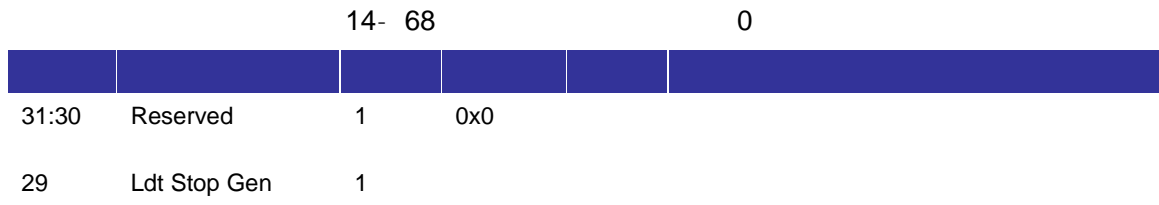
31:16	ht_rx_p2p0_base[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]
15:0	ht_rx_p2p0_mask[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]

14- 66 HT P2P 1

31	ht_rx_p2p1_en	1	0x0	R/W	HT	P2P	1	
29:0	ht_rx_p2p1_trans[53:24]	30	0x0	R/W	HT	P2P	1	[53:24]

14- 67 HT P2P 1

31:16	ht_rx_p2p1_base[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]
15:0	ht_rx_p2p1_mask[39:24]	16	0x0	R/W	HT	P2P	1	[39:24]



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					0xF
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14- 69

1

31	tx post split en	1	0x0	R/W																																																	
30	tx wr passPW pc	1	0x0	R/W																																																	
29	tx wr passPW npc	1	0x0	R/W																																																	
28	tx rd passPW	1	0x0	R/W																																																	
27	stop same id wr	1	0x0	R/W																																																	
26	stop same id rd	1	0x0	R/W																																																	
25	Not axi2seqid wr	1	0x0	R/W																																																	
24	Not axi2seqid rd	1	0x0	R/W																																																	
23:22	Reserved	2	0x0	R/W																																																	
21	act as slave	1	0x1	R/W																																																	
20	Host hide	1	0x0	R/W																																																	
19:16	Rrequest delay	4	0x3	R/W	<div style="text-align: right; padding-right: 20px;">Rrequest</div> <table style="width: 100%; border: none;"> <tr><td style="width: 10%;">000</td><td style="width: 10%;">0</td><td style="width: 10%;"></td><td style="width: 10%;"></td><td style="width: 10%;"></td><td style="width: 10%;"></td></tr> <tr><td>001</td><td></td><td>0-8</td><td></td><td></td><td></td></tr> <tr><td>010</td><td></td><td>8-15</td><td></td><td></td><td></td></tr> <tr><td>011</td><td></td><td>16-31</td><td></td><td></td><td></td></tr> <tr><td>100</td><td></td><td>32-63</td><td></td><td></td><td></td></tr> <tr><td>101</td><td></td><td>64-127</td><td></td><td></td><td></td></tr> <tr><td>110</td><td></td><td>128-255</td><td></td><td></td><td></td></tr> <tr><td>111</td><td></td><td>0</td><td></td><td></td><td></td></tr> </table>	000	0					001		0-8				010		8-15				011		16-31				100		32-63				101		64-127				110		128-255				111		0			
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100		32-63																																																			
101		64-127																																																			
110		128-255																																																			
111		0																																																			

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15	Crc Int en	1	0x0	R/W																																																																									
14:12	Crc Int route	3	0x0	R/W																																																																									
11	Reserved																																																																												
10	ht int 8 bit	1	0x0	R/W																																																																									
9:8	ht_int_stripe	2	0x0	R/W	3 0x0 ht_int_stripe_1 0x1 ht_int_stripe_2 0x2 ht_int_stripe_4																																																																								
4:0	Interrupt Index	5	0x0	R/W	<table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td></td> <td></td> <td>SMI</td> <td>NMI</td> <td>INIT</td> </tr> <tr> <td>INTA</td> <td>INTB</td> <td>INTC</td> <td>INTD</td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td>256</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> <td>5</td> </tr> <tr> <td>000</td> <td></td> <td></td> <td>SMI</td> <td></td> <td></td> </tr> <tr> <td>001</td> <td></td> <td></td> <td>NMI</td> <td></td> <td></td> </tr> <tr> <td>010</td> <td></td> <td></td> <td>INIT</td> <td></td> <td></td> </tr> <tr> <td>011</td> <td></td> <td></td> <td>Reserved</td> <td></td> <td></td> </tr> <tr> <td>100</td> <td></td> <td></td> <td>INTA</td> <td></td> <td></td> </tr> <tr> <td>101</td> <td></td> <td></td> <td>INTB</td> <td></td> <td></td> </tr> <tr> <td>110</td> <td></td> <td></td> <td>INTC</td> <td></td> <td></td> </tr> <tr> <td>111</td> <td></td> <td></td> <td>INTD</td> <td></td> <td></td> </tr> </table>				SMI	NMI	INIT	INTA	INTB	INTC	INTD								256						5	000			SMI			001			NMI			010			INIT			011			Reserved			100			INTA			101			INTB			110			INTC			111			INTD		
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110			INTC																																																																										
111			INTD																																																																										

14- 70

31:16	rx_cad_phase_0	16	0x0	R/W	CAD[15:0]															
15:8	rx_ctl_catch	8	0x0	R/W	<table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td></td> <td></td> <td></td> <td>ctl</td> </tr> <tr> <td>0</td> <td>2</td> <td>4</td> <td>6</td> <td>CIL0</td> </tr> <tr> <td>1</td> <td>3</td> <td>5</td> <td>7</td> <td>CIL1</td> </tr> </table>					ctl	0	2	4	6	CIL0	1	3	5	7	CIL1
				ctl																
0	2	4	6	CIL0																
1	3	5	7	CIL1																
7:0																				

14- 71 PHY

31:29	Reserved	3	0x0	R	
28	dll locked hi	1	0x0	R	
27	dll locked lo	1	0x0	R	
26	cdr locked hi	1	0x0	R	
25	cdr locked lo	1	0x0	R	
24	phase locked	1	0x0	R	
23:20	phy state	4	0x0	R	
19:17	tx training status	3	0x0	R	
16:14	rx training status	3	0x0	R	
13:8	Init done	6	0x0	R	
7:0	Reserved	8		R	

14- 72

31:24	B_CMD_txbuffer	8	0x0	R	B
23:16	R_CMD_txbuffer	8	0x0	R	R
15:8	NPC_CMD_txbuffer	8	0x0	R	NPC
7:0	PC_CMD_txbuffer	8	0x0	R	PC

14- 73

31	Reserved	1	0x0	R	
30	rx_buffer_r_data[4]	1	0x0	R/W	buffer
29	rx_buffer_npc_data[4]	1	0x0	R/W	npc buffer
28	rx_buffer_pc_data[4]	1	0x0	R/W	pc buffer
27	rx_buffer_b_cmd[4]	1	0x0	R/W	bresponse buffer
26	rx_buffer_r_cmd[4]	1	0x0	R/W	buffer
25	rx_buffer_npc_cmd[4]	1	0x0	R/W	npc buffer
24	rx_buffer_pc_cmd[4]	1	0x0	R/W	pc buffer
23:16	R_DATA_txbuffer	8	0x0	R	R
15:8	NPC_DATA_txbuffer	8	0x0	R	NPC
7:0	PC_DATA_txbuffer	8	0x0	R	PC

14- 74

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31	b_interleave	1	0x0	R/W	
30	nop_interleave	1	0x0	R/W	
29	Tx_neg	1	0x0	R/W	0 1 +1
28	Tx_buff_adj_en	1	0x0	R/W	0->1
27:24	R_DATA_txadj	4	0x0	R/W	R tx_neg 0 R_DATA_txadj tx_neg 1 R_DATA_txadj+1
23:20	NPC_DATA_txadj	4	0x0	R/W	NPC tx_neg 0 NPC_DATA_txadj tx_neg 1 NPC_DATA_txadj+1
19:16	PC_DATA_txadj	4	0x0	R/W	PC tx_neg 0 PC_DATA_txadj tx_neg 1 PC_DATA_txadj+1
15:12	B_CMD_txadj	4	0x0	R/W	B tx_neg 0 B_CMD_txadj tx_neg 1 B_CMD_txadj+1
11:8	R_CMD_txadj	4	0x0	R/W	R tx_neg 0 R_CMD_txadj tx_neg 1 R_CMD_txadj+1
7:4	NPC_CMD_txadj	4	0x0	R/W	NPC / tx_neg 0 NPC_CMD_txadj tx_neg 1 NPC_CMD_txadj+1
3:0	PC_CMD_txadj	4	0x0	R/W	PC tx_neg 0 PC_CMD_txadj tx_neg 1 PC_CMD_txadj+1

14- 75

27:24	rx_buffer_r_data	4	0x0	R/W	buffer
23:20	rx_buffer_npc_data	4	0x0	R/W	npc buffer
19:16	rx_buffer_pc_data	4	0x0	R/W	pc buffer
15:12	rx_buffer_b_cmd	4	0x0	R/W	bresponse buffer
11:8	rx_buffer_r_cmd	4	0x0	R/W	buffer
7:4	rx_buffer_npc_cmd	4	0x0	R/W	npc buffer
3:0	rx_buffer_pc_cmd	4	0x0	R/W	pc buffer

14- 76 Training 0

31	Gen3_timing_soft	1	0x0	R/W	
30:23	Retry_nop_num	8	0x0	R/W	
22:0	T0time	23	0x80	R/W	Training 0

14- 77 Training 0



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31:0	T0 time	32	0xffff	R/W	Training 0

14- 78 Training 1



31:0	T1 time	32	0x4ffff	R/W	Training 1
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3C500L					
31:0	T3time	32	0x7ffff	R/W	Training 3

14- 81

31	27	PLLrelock counter	5	0x0	R/W
26		Counter select	1	0x0	R/W
25		Reserved	1	0x0	R
24	16	Soft_div_loop	7	0x0	R/W
15	12	Soft_div_refc	4	0x0	R/W
11	8	Soft_phy_hi_div	4	0x0	R/W
7	4	Soft_phy_lo_div	4	0x0	R/W
3		Locked	1	0x0	R
2		Reserved	1	0x0	R
1		Soft config enable	1	0x0	R/W
0		Reserved	1	0x0	R

14- 82

31		Tx_scanin_en	1	0x0	R/W TX
30		Rx_scanin_en	1	0x0	R/W RX
27:24		Tx_scanin_ncode	4	0x0	R/W TX ncode

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23:20	Tx_scanin_pcode	4	0x0	R/W	TX	pcode
19:12	Rx_scanin_code	8	0x0	R/W	RX	

14- 83 PHY

31	Rx_ckpll_term	1	0x1	R/W	PLL	RX
30	Tx_ckpll_term	1	0x0	R/W	PLL	TX
29	Rx_clk_in_sel_	1	0x0	R/W	PAD	PAD HT1
CLKPAD:						
1'b0						
1'b1 PLL						
28	Rx_ckdll_sell	1	0x0	R/W		DLL
1'b0 PLL						
1'b1						
27:26	Rx_ctle_bitc	2	0x0	R/W	PADEQD	
25:24	Rx_ctle_bitr	2	0x3	R/W	PADEQD	
23:22	Rx_ctle_bitlim	2	0x0	R/W	PADEQD	
21	Rx_om_i					

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16:12	Tx_preenmp	5	0x08	R/W	PAD
11:0	Reserved	12	0x0	R	

14- 84

15	Cdr_ignore_enable	1	0x0	R/W	
14:0	Cdr_wait_counter	15	0x0	R/W	

14- 85 LDT 1

31:16	Rx_wait_time	16	0x0	R/W	RX
15:0	Tx_wait_time	16	0x0	R/W	TX

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14- 90 LDT

5

31:0	wait cad	32	0x0	R/W	

14- 91 HT TX POST ID WIN0

31:16	HT TX POST ID0 MASK	16	0x0	R/W	
15:0	HT TX POST ID0 BASE	16	0x0	R/W	

14- 92 HT TX POST ID WIN1

31:16	HT TX POST ID1 MASK	16	0x0	R/W	
15:0	HT TX POST ID1 BASE	16	0x0	R/W	

14- 93 HT TX POST ID WIN2

31:16	HT TX POST ID2 MASK	16	0x0	R/W	

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15:0	HT TX POST ID2 BASE	16	0x0	R/W	
------	---------------------	----	-----	-----	--

14- 94 HT TX POST ID WIN3

31:16	HT TX POST ID3 MASK	16	0x0	R/W	
15:0	HT TX POST ID3 BASE	16	0x0	R/W	

14- 95 HT RX INT TRANS LO

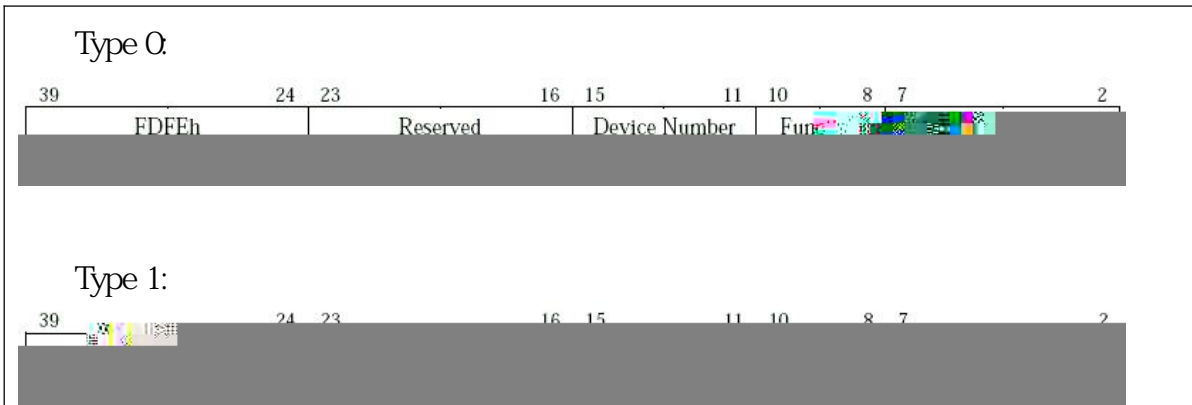
31:4	INT_trans_addr[31:4]	28	0x0	R/W	
3:0	Reserved	4	0x0	R	

14- 96 HT RX INT TRANS Hi

31	INT_trans_en	1	0x0	R/W	
30	INT_trans_allow	1	0x0	R/W	

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29:26	INT_trans_cache	4	0x0	R/W	
25:0	INT_trans_addr[57:32]	26	0x0	R/W	





' /
'
' 16
'
'
' FIFO
' NS16550A
'

[7 0]
0x00
0x00

7:0	Tx FIFO	8	W	

[7 0]

0x01

0x00

7:4	Reserved	4	RW	
3	IME	1	RW	Modem '0' – '1' –
2	ILE	1	RW	'0' – '1' –
1	ITxE	1	RW	'0' – '1' –
0	IRxE	1	RW	'0' – '1' –

[7 0]

0x02

0xc1

7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

Bit 3	Bit 2	Bit 1			
-------	-------	-------	--	--	--

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0	1	1	1st			LSR
0	1	0	2nd		FIFO trigger	FIFO trigger
1	1	0	2nd		FIFO 4	FIFO
0	0	1	3rd			THR IIR
0	0	0	4th	Modem	CTS, DSR, RI or DCD.	MSR

FIFO
[7 0]
0x02
0xc0

7:6	TL	2	W	FIFO trigger '00' – 1 '01' – 4 '10' – 8 '11' – 14
5:3	Reserved	3	W	
2	Txset	1	W	'1' FIFO
1	Rxset	1	W	'1' FIFO

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0	Reserved	1	W	
---	----------	---	---	--

[7 0]

0x03

0x03

Bit	Field Name	Width	Access	Description
7	dlab	1	RW	'1' – '0' –
6	bcb	1	RW	'1' – 0(). '0' –
5	spb	1	RW	'0' – '1' – LCR[4] 1 0 LCR[4] 0 1
4	eps	1	RW	'0' – 1 '1' – 1

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3	pe	1	RW	'0' – '1' –
2	sb	1	RW	'0' – 1 '1' – 5 1.5 2
1:0	bec	2	RW	'00' – 5 '01' – 6 '10' – 7 '11' – 8

Modem

[7 0]

0x04

0x00

7:5	Reserved	3	W	
4	Loop	1	W	'0' – '1' – TXD 1

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				DTR è DSR RTS è CTS Out1 è RI Out2 è DCD
3	OUT2	1	W	DCD
2	OUT1	1	W	RI
1	RTSC	1	W	RTS
0	DTRC	1	W	DTR

[7 0]

0x05

0x00

7	ERROR	1	R	'1' – '0' –
6	TE	1	R	'1' – FIFO

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				FIFO '0' –
5	TFE	1 ↓	R	FIFO '1' – FIFO FIFO '0' –
4	BI	1	R	'1' – 0 '0' –
3	FE	1	R	'1' – '0' –
2	PE	1	R	'1' – '0' –
1	OE	1	R	'1' – '0' –
0	DR	1	R	'0' – FIFO '1' – FIFO

Modem

[7 0]

0x06

0x00

7	CDCD	1	R	DCD	Out2
6	CRI	1	R	RI	OUT1
5	CDSR	1	R	DSR	DTR
4	CCTS	1	R	CTS	RTS
3	DDCD	1	R	DDCD	
2	TERI	1	R	RI	RI
1	DDSR	1	R	DDSR	
0	DCTS	1	R	DCTS	

FIFO

[7 0]

0x08

0x00

--	--	--	--	--	--

3C5000L



0x00

7:0	D_DIV	8	RW	

'
' 4
'
'
'
'
'
'
' SPI
' SPI
' Dual/Quad mode SPI flash

15- 1 SPI

SPI Boot	0X1FC0_0000-0X1FD0_0000	1MByte
SPI Memory	0X1D00_0000-0X1E00_0000	16MByte
SPI Register	0X1FE0_01F0-0X1FE0_01FF	16Byte

[7 0]
0x00
0x10

7	Spie	1	RW		
6	spe	1	RW		
5	Reserved	1	RW		
4	mstr	1	RW	master	1
3	cpol	1	RW		
2	cpha	1	RW	1	0
1:0	spr	2	RW	sclk_o	sper spre

[7 0]

0x01

0x05

7	spif	1	RW	1 1
6	wcol	1	RW	1 , 1
5:4	Reserved	2	RW	
3	wfull	1	RW	1
2	wfempty	1	RW	1
1	rffull	1	RW	1
0	rfempty	1	RW	1

[7 0]

0x02

0x00

7:0	Tx FIFO	8	W	

[7 0]

0x03

0x00

7:6	icnt	2	RW	00 - 1 01 - 2 10 - 3 11 - 3
5:2	Reserved	4	RW	
1:0	spre	2	RW	Spr

spre	00	00	00	00	01	01	01	01	10	10	10	10
spr	00	01	10	11	00	01	10	11	00	01	10	11
	2	4	16	32	8	64	128	256	512	1024	2048	4096

SPI Flash

[7 0]

0x04

0x21

7:4	clk_div	4	RW	{spre,spr}
3	dual_io	1	RW	I/O
2	fast_read	1	RW	
1	burst_en	1	RW	spr flash

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0	memory_en	1	RW	spi flash	csn[0]
---	-----------	---	----	-----------	--------

SPI Flash

[7 0]

0x05

0x00

Field	Name	Width	Access	Value
7:4	csn	4	RW	csn
3:0	csen	4	RW	1 cs 7:4

SPI Flash

[7 0]

0x06

0x03

Field	Name	Width	Access	Value
7:4	Reserved	4	RW	
3	quad_io	1	RW	4 1
2	tFast	1	RW	
1:0	tCSH	2	RW	SPI Flash T 00: 1T 01: 2T 10: 4T 11: 8T

SPI Flash

[7 0]

0x08

0x00

7:4	nbyte	4	RW	
3:2	reserve	2	RW	
1	nbmode	1	RW	
0	start	1	RW	

SPI Flash

[7 0]

0x09

0x00

7:0	cmd	8	RW	spi flash

SPI Flash

0

[7 0]

0x0a

0x00

7:0	buf0	8	RW	SPI SPI

SPI Flash 1
 [7 0]
 0x0b
 0x00

7:0	buf1	8	RW	SPI	SPI
-----	------	---	----	-----	-----

SPI Flash 0
 [7 0]
 0x0c
 0x00

7:0	time0	8	RW	8
-----	-------	---	----	---

SPI Flash 1
 [7 0]
 0x0d
 0x00

7:0	time1	8	RW	8
-----	-------	---	----	---

SPI Flash 2



[7 0]

0x00

0xff

7:0	PRERlo	8	RW	8

[7 0]

3C5000L

0x01

0xff

7:0	PRERhi	8	RW	8
-----	--------	---	----	---

[7 0]

0x02

0x20

7	EN	1	RW	1 , 0
6	IEN	1	RW	1
5	MST_EN	1	RW	0 slave 1 master
4:0	Reserved	5	RW	

[7 0]

0x03

0x00

7:1	DATA	7	W	
0	DRW	1	W	

[7 0]

0x03

0x00

7:0	RXR	8	R	

[7 0]

0x04

0x00

7	STA	1	W	START
6	STO	1	W	STOP
5	RD	1	W	
4	WR	1	W	
3	ACK	1	W	
2:1	Reserved	2	W	
0	IACK	1	W	

[7 0]

0x04

0x00

7	RxACK	1	R	1



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				0
6	Busy	1	R	I2c 1 0
5	AL	1	R	I2C I2C 1
4:2	Reserved	3	R	
1	TIP	1	R	1 0
0	IF	1	R	1

[7 0]

0x07

0x00

7	SLV_EN	1	WR	MST_EN 0
6 0	SLV_ADDR	7	WR	I2C